PCN Number:	20160125000	**PCN Date:**	01/28/2016
Title:	Datasheet update DS90UH940-Q1/DS90UB940-Q1/DS90UH948-Q1/ DS90UB948-Q1		
Customer Contact:	PCN Manager	**Dept:**	Quality Services
Proposed 1st Ship Date:	07/28/2016		
Change Type:			

☐	Assembly Site	☐	Design	☐	Wafer Bump Site
☐	Assembly Process	☒	Data Sheet	☐	Wafer Bump Material
☐	Assembly Materials	☐	Part number change	☐	Wafer Bump Process
☐	Mechanical Specification	☐	Test Site	☐	Wafer Fab Site
☐	Packing/Shipping/Labeling	☐	Test Process	☐	Wafer Fab Materials
				☐	Wafer Fab Process

PCN Details

Description of Change:

The product datasheet(s) is being updated as summarized below.

The following change history provides further details.

TEXAS INSTRUMENTS

DS90UH940-Q1

SNLS478A – NOVEMBER 2014 – REVISED JANUARY 2016 www.ti.com

Changes from Original (November 2014) to Revision A **Page**

- Added shared pins description on SPI pins 5
- Added shared pins description on GPIO pins 6
- Added shared pins description on D_GPIO pins 6
- Added shared pins description on register only GPIO pins. Changed "Local register control only" to "I2C register control only". 6
- Added shared pins description on slave mode I2S pins 7
- Added shared pins description on master mode I2S pins 7
- Added legend on I/O TYPE 8
- Moved Storage Temperature Range from ESD to Absolute Maximum Ratings table 9
- Added ESD Ratings table. 9
- Changed IDD12Z limit from 11mA to 30mA per PE re-characterization 12
- Changed Fast Plus Mode t_{SP} maximum from 20ns to 50ns 14
- Added Power Sequence section 22
- Deleted MODE, CSI LANE, REPLICATE columns in MODE_SEL0 table 40
- Deleted MODE column. Added (CSI PORT) to CSI_SEL column in MODE_SEL1 table. 40
- Changed default value from "0" to "1" in register 0x01[2] 47
- Added description to register 0x01[1] "Registers which are loaded by pin strap will be restored to their original strap value when this bit is set. These registers show 'Strap' as their default value in this table." 47
- Added to 0x02[7] in Description column "A Digital reset 0x01[0] should be asserted after toggling Output Enable bit *LOW* to *HIGH*" 47
- Added "Loaded from remote SER" in register 0x07[7:1] function column. 49
- Changed signal detect bit to reserved in register 0x1C[1] 52
- Changed "0" to "0/1" in register RW column of 0x1C[1] 52

Changes from Original (November 2014) to Revision A **Page**

- Added shared pins description on SPI pins 5
- Added shared pins description on GPIO pins 6
- Added shared pins description on D_GPIO pins 6
- Added shared pins description on register only GPIO pins. Changed "Local register control only" to "I2C register control only". 6
- Added shared pins description on slave mode I2S pins 7
- Added shared pins description on master mode I2S pins 7
- Added legend on I/O TYPE 8
- Moved Storage Temperature Range from ESD to Absolute Maximum Ratings table 9
- Added ESD Ratings table. 9
- Changed IDD12Z limit from 11mA to 30mA per PE re-characterization 12
- Changed Fast Plus Mode t_{SP} maximum from 20ns to 50ns 14
- Added Power Sequence section 22
- Deleted MODE, CSI LANE, REPLICATE columns in MODE_SEL0 table 39
- Deleted MODE column. Added (CSI PORT) to CSI_SEL column in MODE_SEL1 table. 39
- Changed default value from "0" to "1" in register 0x01[2] 46
- Added description to register 0x01[1] "Registers which are loaded by pin strap will be restored to their original strap value when this bit is set. These registers show 'Strap' as their default value in this table." 46
- Added to 0x02[7] in Description column "A Digital reset 0x01[0] should be asserted after toggling Output Enable bit *LOW* to *HIGH*" 46
- Added "Loaded from remote SER" in register 0x07[7:1] function column 48
- Changed signal detect bit to reserved in register 0x1C[1] 51
- Changed "0" to "0/1" in register RW column of 0x1C[1] 51

Changes from Original (October 2014) to Revision A **Page**

- Added shared pins description on SPI pins 5
- Added shared pins description on GPIO pins 6
- Added shared pins description on D_GPIO pins 6
- Added shared pins description on register only GPIO pins. Changed "Local register control only" to "I2C register control only". 6
- Added shared pins description on slave mode I2S pins 7
- Added shared pins description on master mode I2S pins 7
- Added legend on I/O TYPE 8
- Moved Storage Temperature Range from ESD to Absolute Maximum Ratings table 9
- Added ESD Ratings table. 9
- Changed V_{OS} from 1.0V to 1.125V 12
- Changed V_{OS} from 1.5V to 1.375V 12
- Changed IDD12Z limit from 8mA to 30mA per PE re-characterization 12
- Changed Fast Plus Mode t_{SP} maximum from 20ns to 50ns 14
- Added Power Sequence section 19
- Added Image Enhancement Features section 44
- Changed default value from "0" to "1" in register 0x01[2] 50
- Added description to register 0x01[1] "Registers which are loaded by pin strap will be restored to their original strap value when this bit is set. These registers show 'Strap' as their default value in this table." 50
- Added to 0x02[7] in Description column "A Digital reset 0x01[0] should be asserted after toggling Output Enable bit *LOW* to *HIGH*" 50
- Added "Loaded from remote SER" in register 0x07[7:1] function column 52
- Changed signal detect bit to reserved 55

Changes from Original (October 2014) to Revision A **Page**

- Added shared pins description on SPI pins 5
- Added shared pins description on GPIO pins 6
- Added shared pins description on D_GPIO pins 6
- Added shared pins description on register only GPIO pins. Changed "Local register control only" to "I2C register control only". 6
- Added shared pins description on slave mode I2S pins 7
- Added shared pins description on master mode I2S pins 7
- Added legend on I/O TYPE 8
- Moved Storage Temperature Range from ESD to Absolute Maximum Ratings table 9
- Added ESD Ratings table. 9
- Changed V_{OS} from 1.0V to 1.125V 12
- Changed V_{OS} from 1.5V to 1.375V 12
- Changed IDD12Z limit from 8mA to 30mA per PE re-characterization 12
- Changed Fast Plus Mode t_{SP} maximum from 20ns to 50ns 14
- Added Power Sequence section 19
- Added Image Enhancement Features section 44
- Changed default value from "0" to "1" in register 0x01[2] 50
- Added description to register 0x01[1] "Registers which are loaded by pin strap will be restored to their original strap value when this bit is set. These registers show 'Strap' as their default value in this table." 50
- Added to 0x02[7] in Description column "A Digital reset 0x01[0] should be asserted after toggling Output Enable bit *LOW* to *HIGH*" 50
- Added "Loaded from remote SER" in register 0x07[7:1] function column 52
- Changed signal detect bit to reserved 55

The datasheet number will be changing.

Device Family	Change From:	Change To:
DS90UH940-Q1	SNLS478	**SNLS478A**
DS90UB940-Q1	SNLS479	**SNLS479A**
DS90UH948-Q1	SNLS473	**SNLS473A**
DS90UB948-Q1	SNLS477	**SNLS477A**

These changes may be reviewed at the datasheet links provided.
http://www.ti.com/product/ds90uh940-q1
http://www.ti.com/product/ds90ub940-q1
http://www.ti.com/product/ds90uh948-q1
http://www.ti.com/product/ds90ub948-q1

Reason for Change:
To more accurately reflect device characteristics.
Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):
Electrical specification performance changes as indicated above.
Changes to product identification resulting from this PCN:
None.
Product Affected:

DS90UB940TNKDRQ1	DS90UB948TNKDRQ1	DS90UH940TNKDRQ1	DS90UH948TNKDRQ1
DS90UB940TNKDTQ1	DS90UB948TNKDTQ1	DS90UH940TNKDTQ1	DS90UH948TNKDTQ1

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

Location	**E-Mail**
USA	PCNAmericasContact@list.ti.com
Europe	PCNEuropeContact@list.ti.com
Asia Pacific	PCNAsiaContact@list.ti.com
Japan	PCNJapanContact@list.ti.com