BUD42D

High Speed, High Gain Bipolar NPN Transistor with Antisaturation Network and Transient Voltage Suppression Capability

The BUD42D is a state−of−the−art bipolar transistor. Tight dynamic characteristics and lot to lot minimum spread make it ideally suitable for light ballast applications.

Features

- Free−Wheeling Diode Built−In
- Flat DC Current Gain
- Fast Switching Times and Tight Distribution
- “6 Sigma” Process Providing Tight and Reproducible Parameter Spreads
- Epoxy Meets UL 94 V−0 @ 0.125 in
- These Devices are Pb−Free and are RoHS Compliant

Two Versions

- BUD42D−1: Case 369D for Insertion Mode
- BUD42D, BUD42DT4: Case 369C for Surface Mount Mode

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Sustaining Voltage	V_{CEO}	350	Vdc
Collector−Base Breakdown Voltage	V_{CBO}	650	Vdc
Collector−Emitter Breakdown Voltage	V_{CES}	650	Vdc
Emitter−Base Voltage	V_{EBO}	9	Vdc
Collector Current − Continuous	I_C	4.0	Adc
Collector Current − Peak (Note 1)	I_{CM}	8.0	Adc
Base Current − Continuous	I_B	1.0	Adc
Base Current − Peak (Note 1)	I_{BM}	2.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	25 0.2	W W/°C
Operating and Storage Temperature	T_J, T_{stg}	−65 to +150	°C
ESD − Human Body Model	HBM	3B	V
ESD − Machine Model	MM	C	V

TYPICAL GAIN

Typical Gain @ I_C = 1 A, V_{CE} = 2 V	h_{FE}	13	−
Typical Gain @ I_C = 0.3 A, V_{CE} = 1 V	h_{FE}	16	−

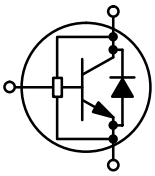
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Pulse Test: Pulse Width = 5.0 ms, Duty Cycle = 10%10

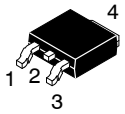
ON Semiconductor®

http://onsemi.com

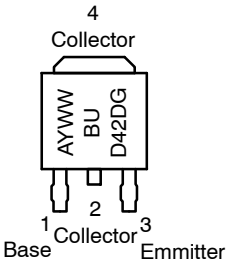
4 AMPERES 650 VOLTS, 25 WATTS POWER TRANSISTOR

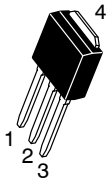


MARKING DIAGRAMS

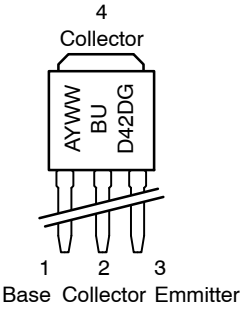


DPAK
CASE 369C
STYLE 1





DPAK
CASE 369D
STYLE 1



A	= Assembly Location
Y	= Year
WW	= Work Week
BUD43D	= Device Code
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

August, 2013 − Rev. 6

Publication Order Number:
BUD42D/D

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	5.0	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	71.4	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8 in from Case for 5 seconds	T_L	260	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector−Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)		$V_{CEO(sus)}$	350	430	–	Vdc
Collector−Base Breakdown Voltage (I_{CBO} = 1 mA)		V_{CBO}	650	780	–	Vdc
Emitter−Base Breakdown Voltage (I_{EBO} = 1 mA)		V_{EBO}	9.0	12	–	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CEO}	– –	– –	100 200	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CES}	– –	– –	10 200	μAdc
Emitter−Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)		I_{EBO}	–	–	100	μAdc
ON CHARACTERISTICS						
Base−Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.2 Adc)		$V_{BE(sat)}$	–	0.85	1.2	Vdc
Collector−Emitter Saturation Voltage (I_C = 2 Adc, I_B = 0.5 Adc)		$V_{CE(sat)}$	–	0.2	1.0	Vdc
DC Current Gain (I_C = 1 Adc, V_{CE} = 2 Vdc) (I_C = 2 Adc, V_{CE} = 5 Vdc)		h_{FE}	8.0 10	13 12	– –	–
DIODE CHARACTERISTICS						
Forward Diode Voltage (I_{EC} = 1.0 Adc)		V_{EC}	–	0.9	1.5	V
SWITCHING CHARACTERISTICS: Resistive Load (D.C.≤ 10%, Pulse Width = 40 μs)						
Turn−Off Time (I_C = 1.2 Adc, I_{B1} = 0.4 A, I_{B2} = 0.1 A, V_{CC} = 300 V)		T_{off}	4.6	–	6.55	μs
Fall Time (I_C = 2.5 Adc, I_{B1} = I_{B2} = 0.5 A, V_{CC} = 150 V, V_{BE} = −2 V)		T_f	–	–	0.8	μs
DYNAMIC SATURATION VOLTAGE						
Dynamic Saturation Voltage: Determined 1 μs and 3 μs respectively after rising I_{B1} reaches 90% of final I_{B1}	I_C = 400 mA, I_{B1} = 40 mA, V_{CC} = 300 V	@ 1 μs	@ T_C = 25°C @ T_C = 125°C	$V_{CE(dsat)}$	– –	2.8 3.2	– –	V
		@ 3 μs	@ T_C = 25°C @ T_C = 125°C		– –	0.75 1.3	– –	
	I_C = 1 A, I_{B1} = 200 mA, V_{CC} = 300 V	@ 1 μs	@ T_C = 25°C @ T_C = 125°C		– –	2.1 4.7	– –	
		@ 3 μs	@ T_C = 25°C @ T_C = 125°C		– –	0.35 0.6	– –	

TYPICAL STATIC CHARACTERISTICS

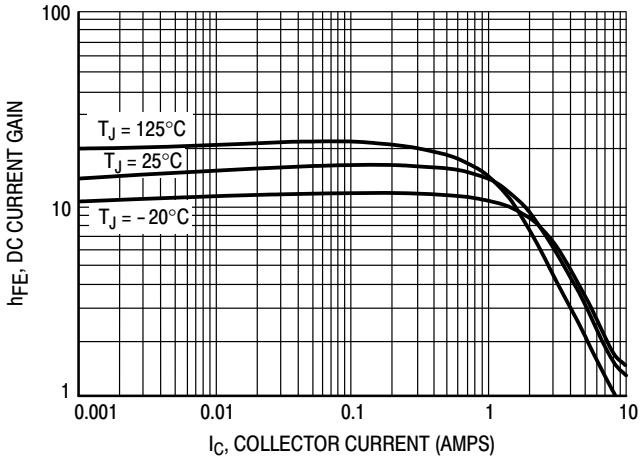


Figure 1. DC Current Gain @ V_{CE} = 1 V

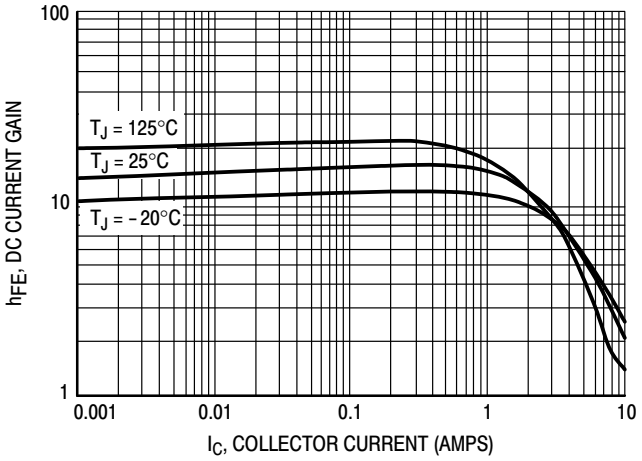


Figure 2. DC Current Gain @ V_{CE} = 5 V

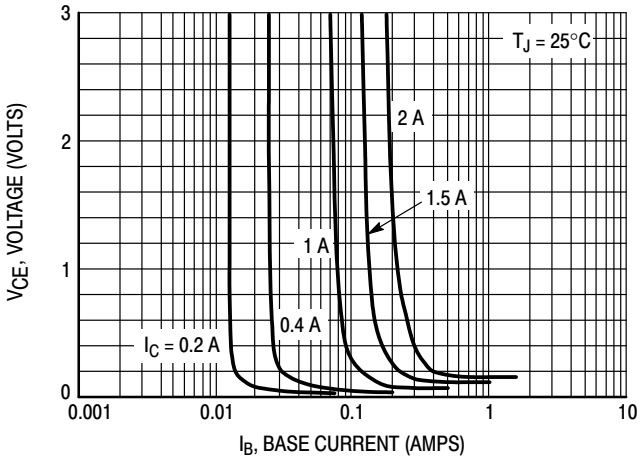


Figure 3. Collector Saturation Region

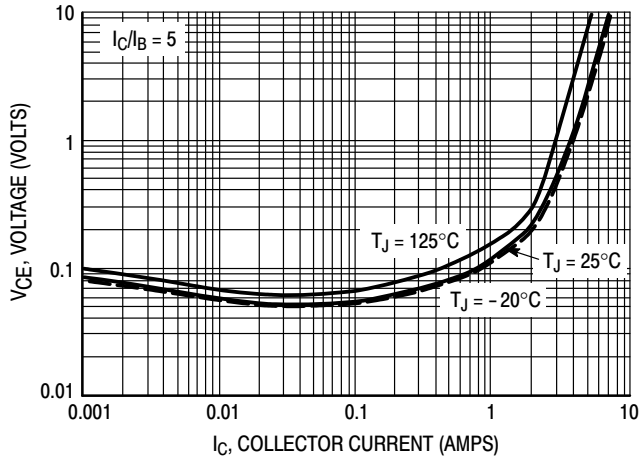


Figure 4. Collector−Emitter Saturation Voltage

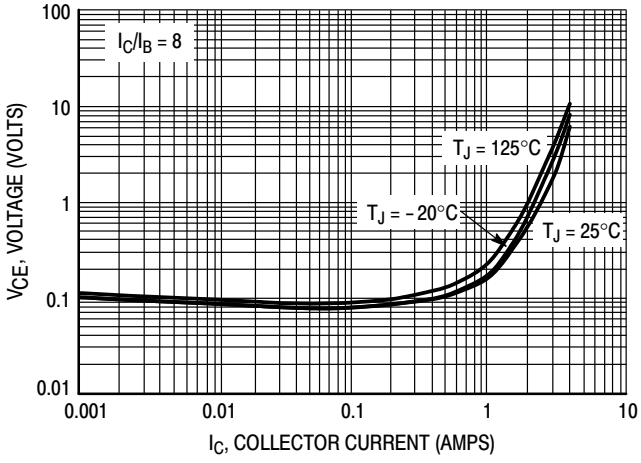


Figure 5. Collector−Emitter Saturation Voltage

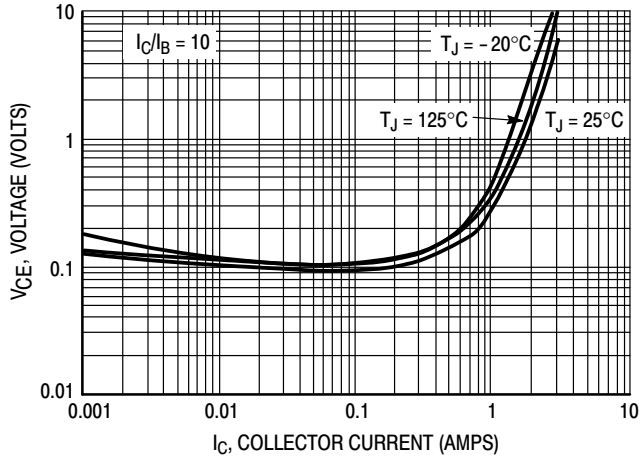


Figure 6. Collector−Emitter Saturation Voltage

TYPICAL STATIC CHARACTERISTICS

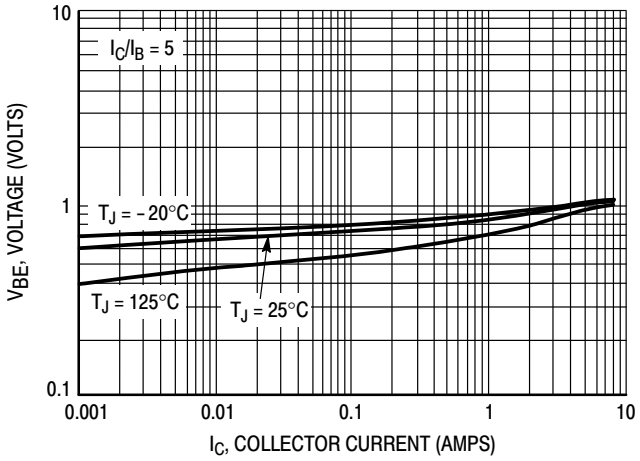


Figure 7. Base−Emitter Saturation Region

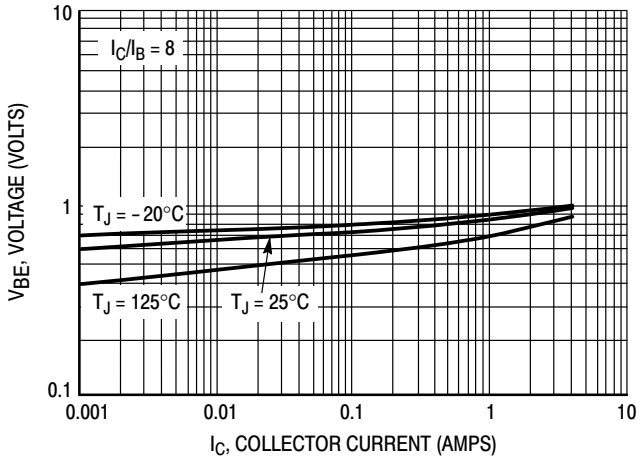


Figure 8. Base−Emitter Saturation Region

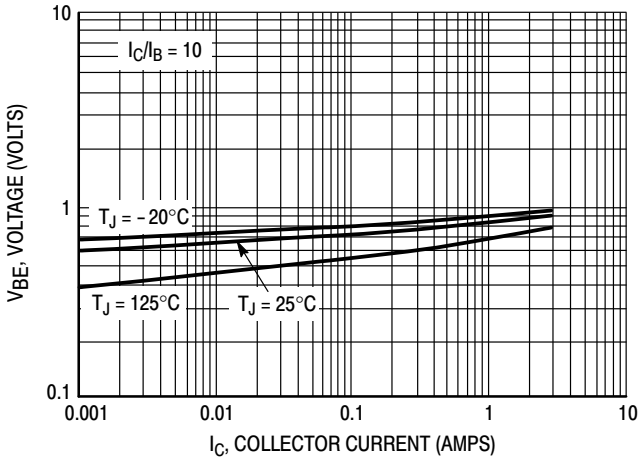


Figure 9. Base−Emitter Saturation Region

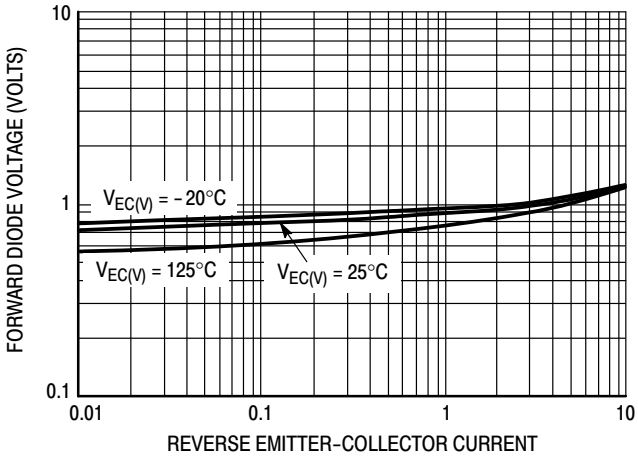


Figure 10. Forward Diode Voltage

TYPICAL SWITCHING CHARACTERISTICS

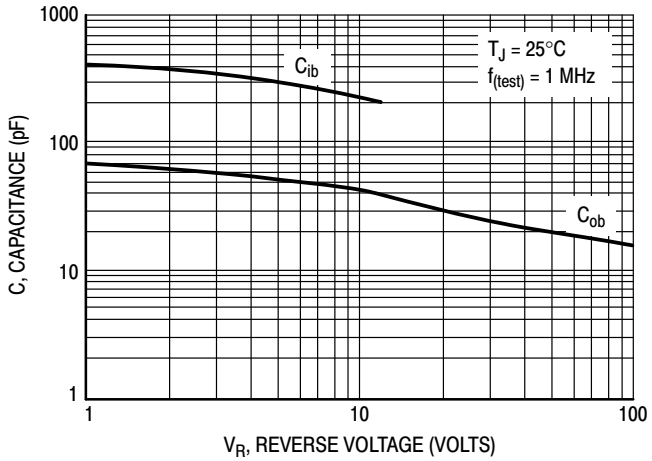


Figure 11. Capacitance

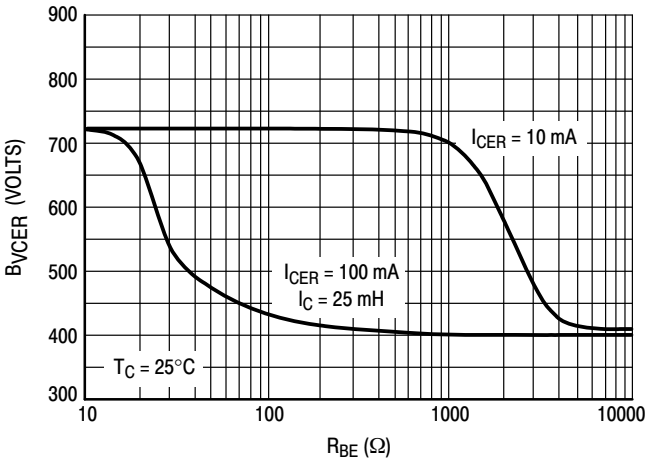


Figure 12. $B_{VCER} = f(R_{BE})$

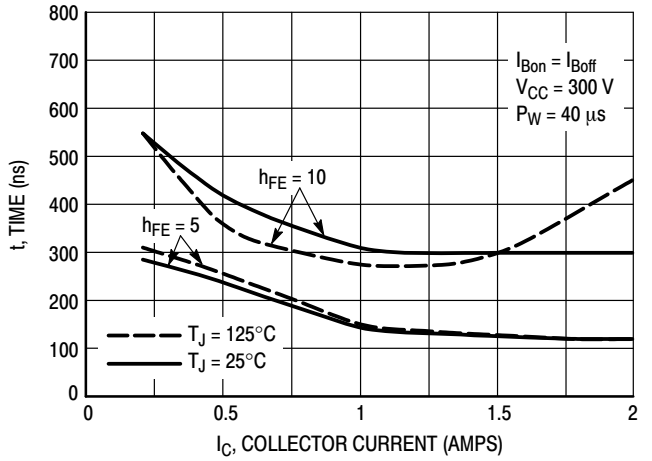


Figure 13. Resistive Switching, t_{on}

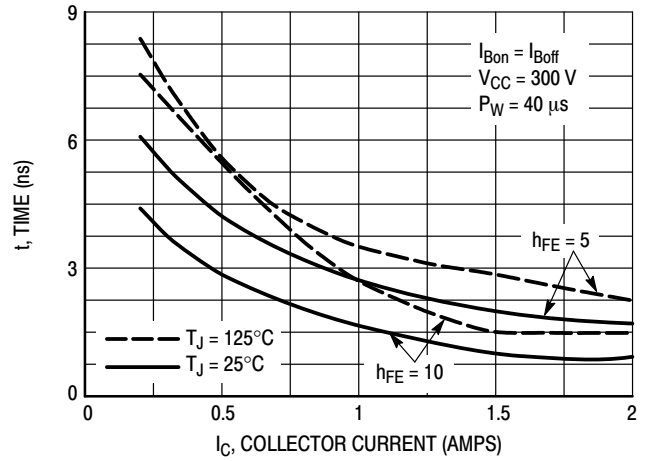


Figure 14. Resistive Switching, t_{off}

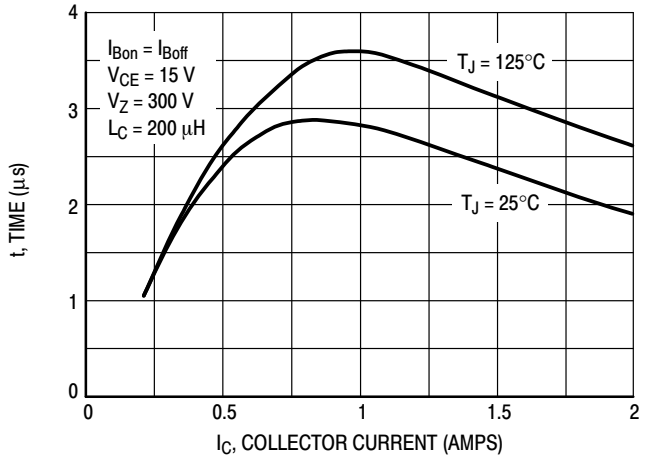


Figure 15. Inductive Storage Time, t_{si} @ h_{FE} = 5

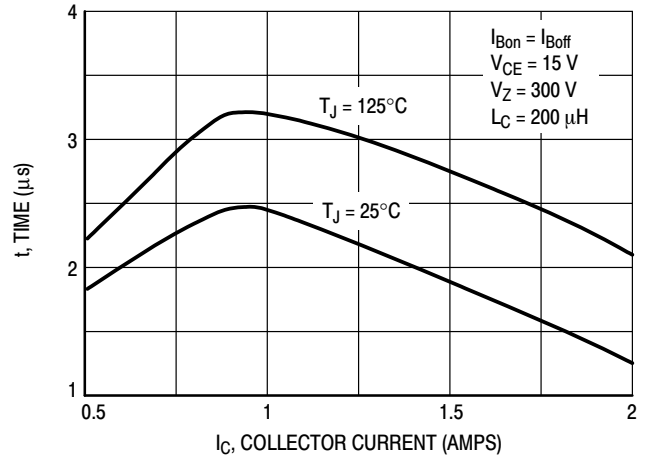


Figure 16. Inductive Storage Time, t_{si} @ h_{FE} = 10

TYPICAL SWITCHING CHARACTERISTICS

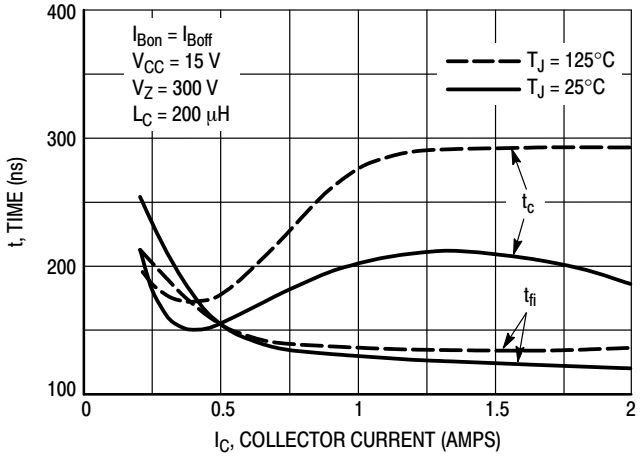


Figure 17. Inductive Fall and Cross Over Time, t_{fi} and t_c @ h_{FE} = 5

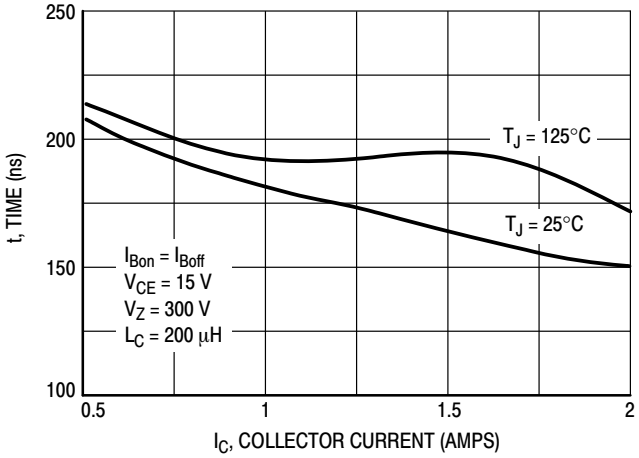


Figure 18. Inductive Fall Time, t_{fi} @ h_{FE} = 10

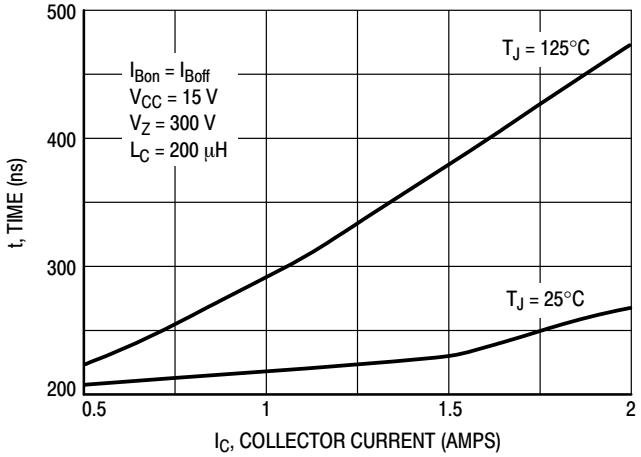


Figure 19. Inductive Cross Over Time, t_c @ h_{FE} = 10

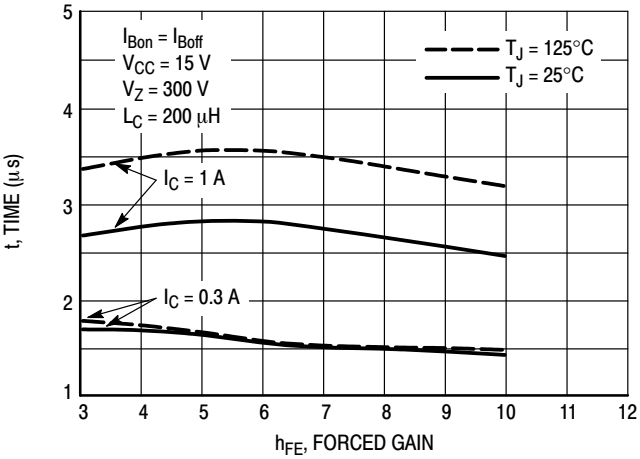


Figure 20. Inductive Storage Time, t_{si}

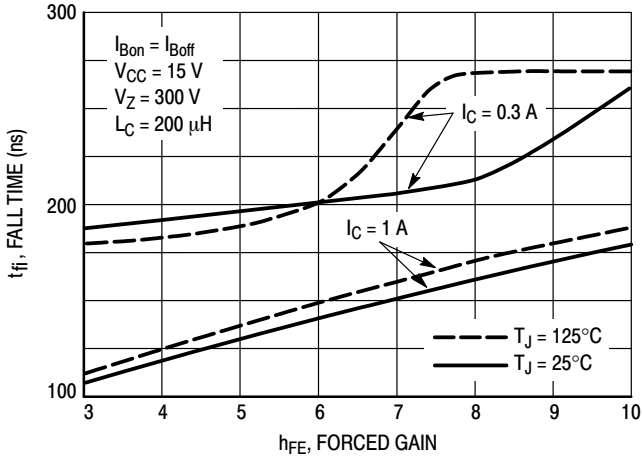


Figure 21. Inductive Fall Time, t_f

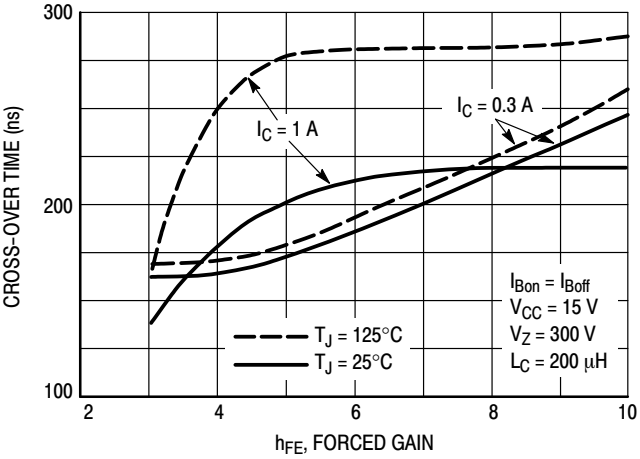


Figure 22. Inductive Cross Over Time, t_c

TYPICAL SWITCHING CHARACTERISTICS

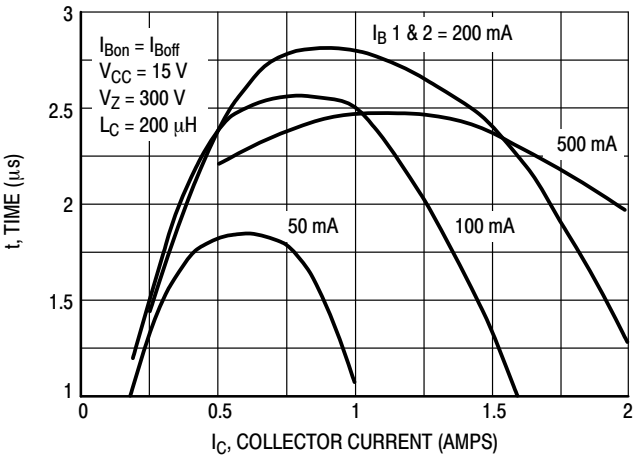


Figure 23. Inductive Storage Time, t_{si}

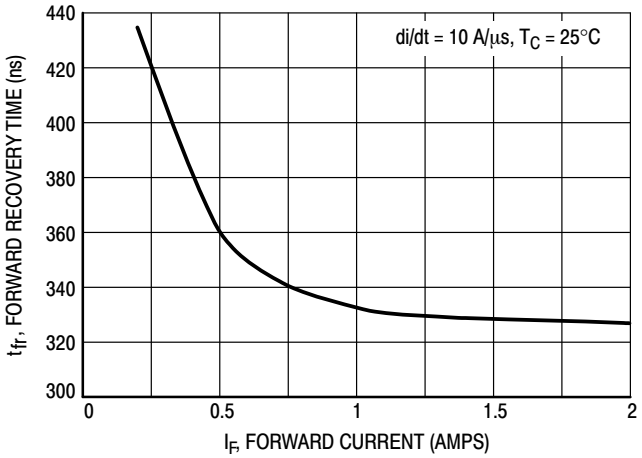


Figure 24. Forward Recovery Time, t_{fr}

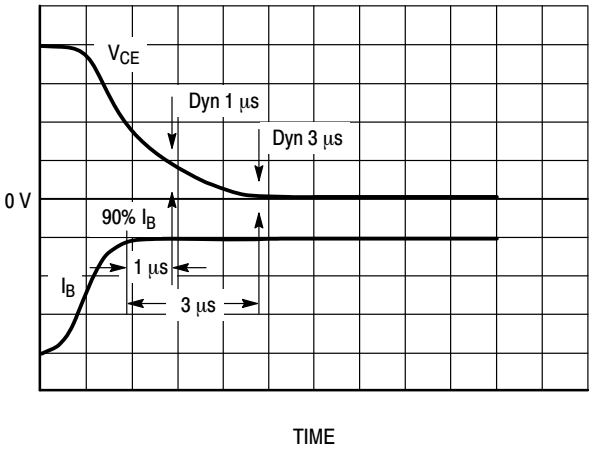


Figure 25. Dynamic Saturation Voltage Measurements

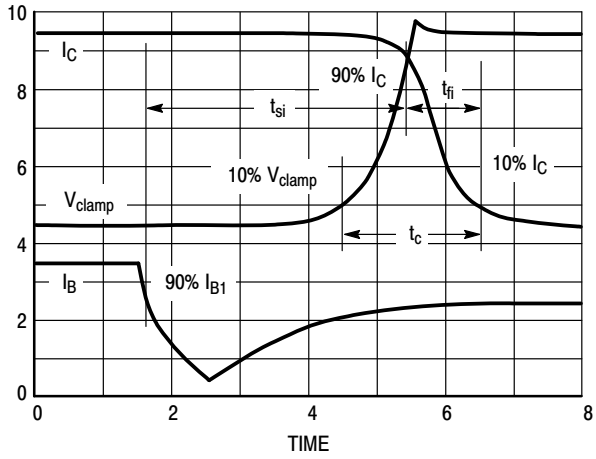
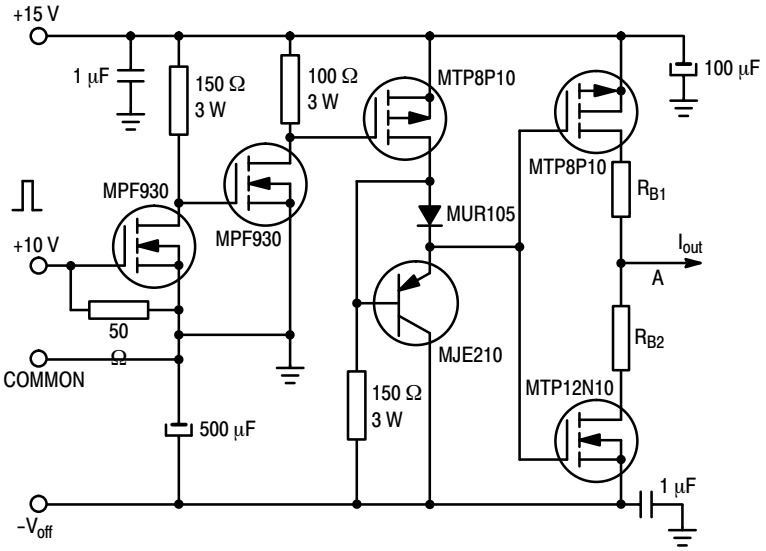
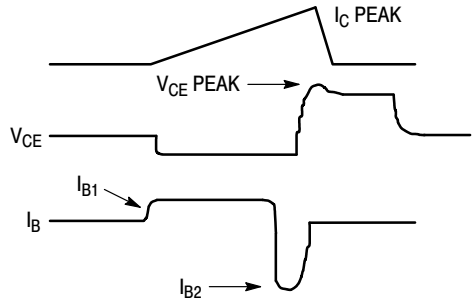


Figure 26. Inductive Switching Measurements

TYPICAL SWITCHING CHARACTERISTICS

Table 1. Inductive Load Switching Drive Circuit





$V_{(BR)CEO(sus)}$	Inductive Switching	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
R_{B2} = ∞	R_{B2} = 0	R_{B2} = 0
V_{CC} = 20 Volts	V_{CC} = 15 Volts	V_{CC} = 15 Volts
$I_{C(pk)}$ = 100 mA	R_{B1} selected for desired I_{B1}	R_{B1} selected for desired I_{B1}

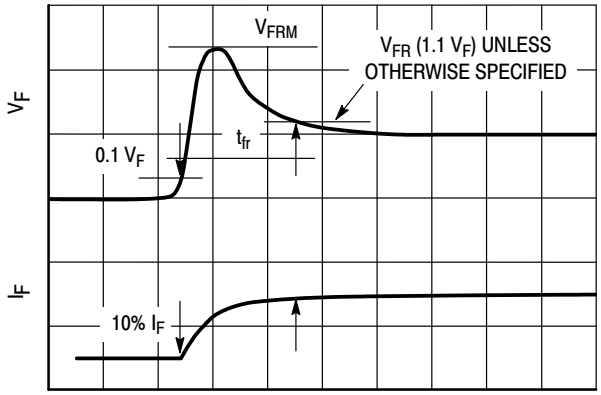


Figure 27. t_{fr} Measurement

MAXIMUM RATINGS

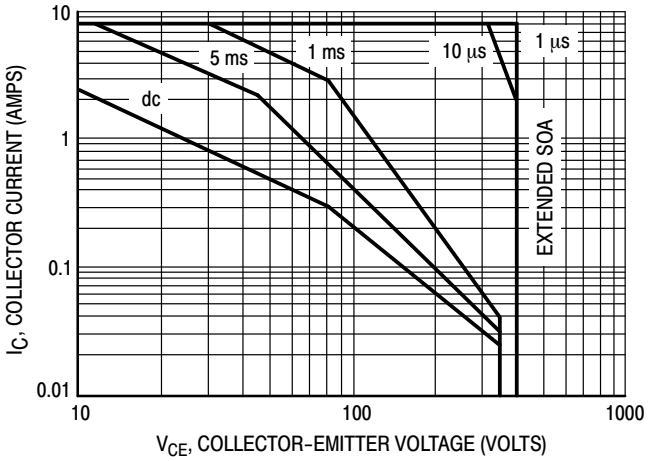


Figure 28. Forward Bias Safe Operating Area

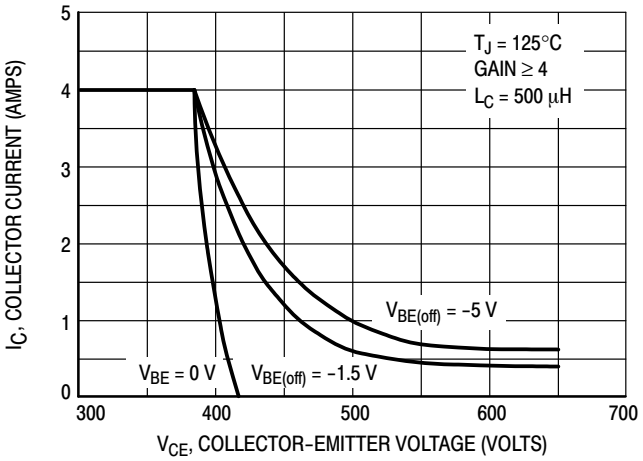


Figure 29. Reverse Bias Safe Operating Area

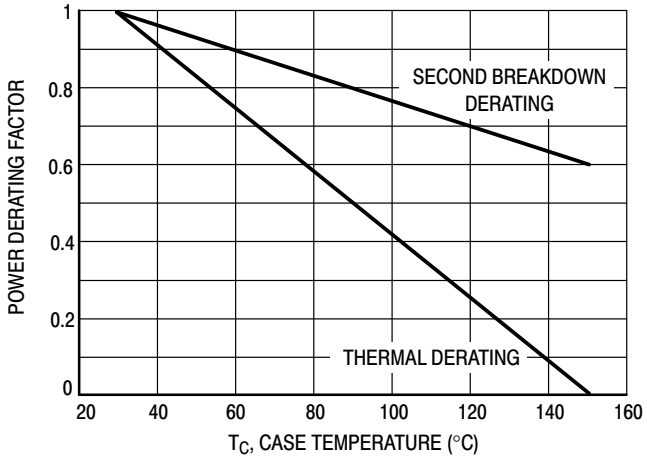


Figure 30. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C−V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 28 is based on T_C = 25°C; $T_{j(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second Breakdown limitations do not derate like thermal limitations. Allowable current at the voltages shown on Figure 28 may be found at any case temperature by using the appropriate curve on Figure 30.

$T_{j(pk)}$ may be calculated from the data in Figure 31. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn−off with the base to emitter junction reverse biased. The safe level is specified as reverse biased safe operating area (Figure 29). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

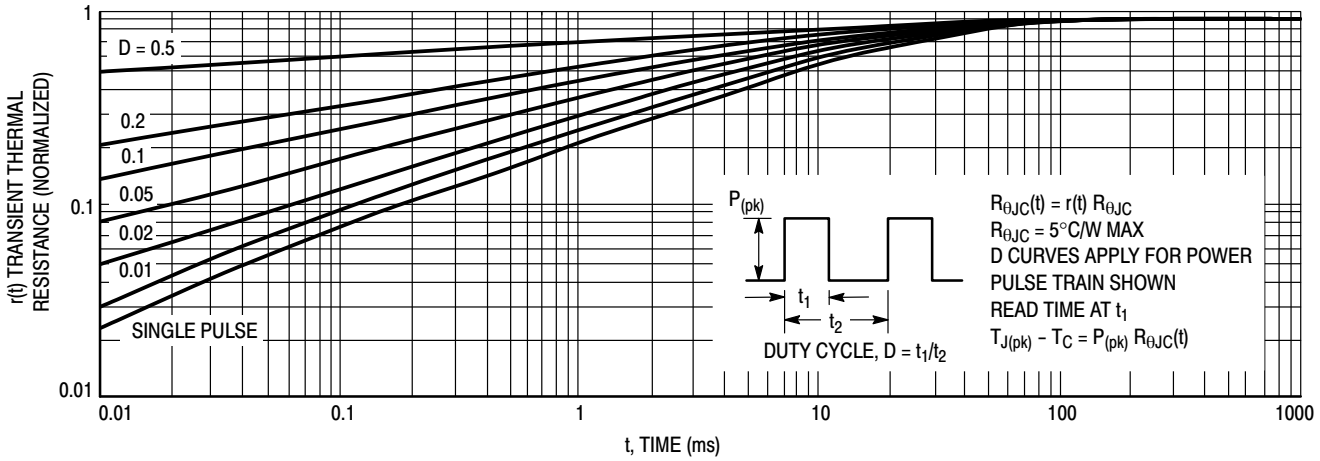


Figure 31. Thermal Response

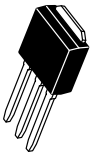
ORDERING INFORMATION

Device	Package	Shipping†
BUD42D−1G	DPAK Straight Lead (Pb−Free)	75 Units / Rail
BUD42DT4G	DPAK (Pb−Free)	2500 Units / Tape & Reel

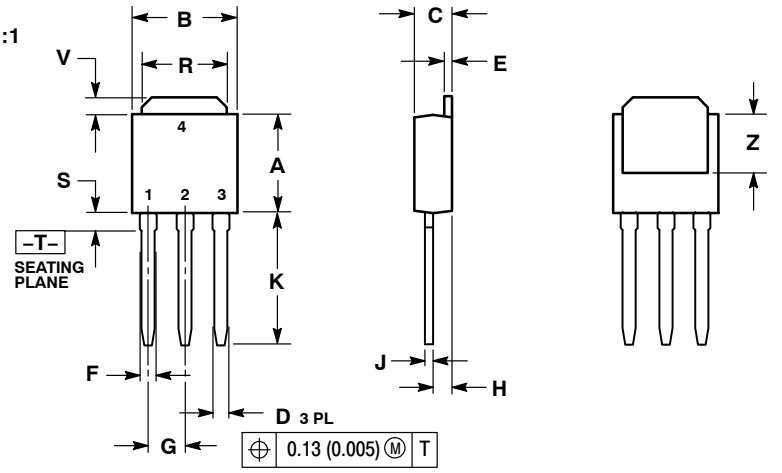
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

IPAK
CASE 369D–01
ISSUE C

DATE 15 DEC 2010



SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

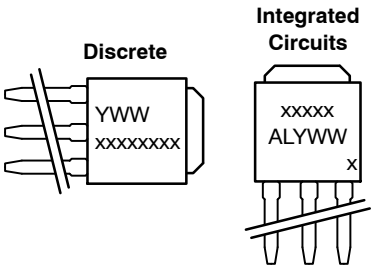
STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

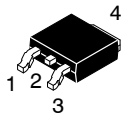
MARKING DIAGRAMS



xxxxxxxxx = Device Code
A = Assembly Location
IL = Wafer Lot
Y = Year
WW = Work Week

DOCUMENT NUMBER:	98AON10528D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	IPAK (DPAK INSERTION MOUNT)	PAGE 1 OF 1

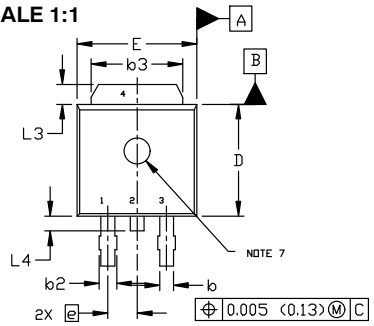
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



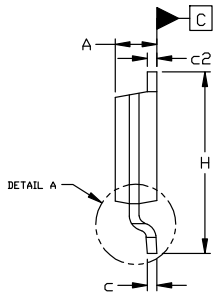
DPAK (SINGLE GAUGE)
CASE 369C
ISSUE G

DATE 31 MAY 2023

SCALE 1:1



TOP VIEW

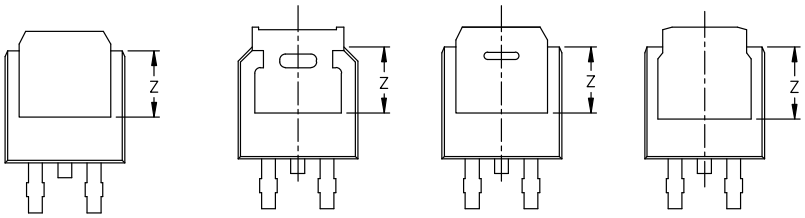


SIDE VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

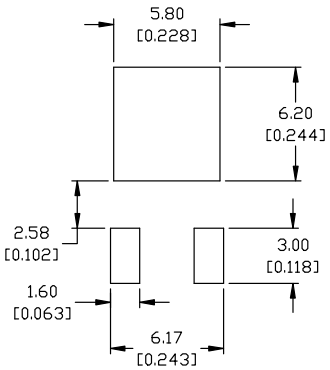
DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	----	0.040	---	1.01
Z	0.155	----	3.93	---



BOTTOM VIEW

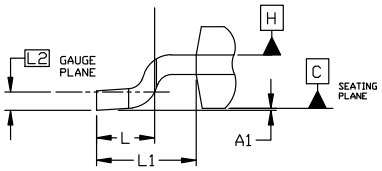
BOTTOM VIEW

ALTERNATE CONSTRUCTIONS



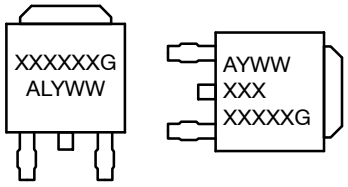
RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.



DETAIL A
ROTATED 90° CW

GENERIC MARKING DIAGRAM*



IC **Discrete**

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

DOCUMENT NUMBER:	**98AON10527D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**DPAK (SINGLE GAUGE)**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales