

PCN Number:	20130716000			PCN Date:	07/31/2013
Title:	DAC3482 Data Sheet				
Customer Contact:	PCN Manager	Phone:	+1(214) 480-6037	Dept:	Quality Services
Proposed 1st Ship Date:	Not Applicable		Estimated Sample Availability:	Not Applicable	
Change Type:					
<input type="checkbox"/>	Assembly Site	<input type="checkbox"/>	Assembly Process	<input type="checkbox"/>	Assembly Materials
<input type="checkbox"/>	Design	<input checked="" type="checkbox"/>	Electrical Specification	<input type="checkbox"/>	Mechanical Specification
<input type="checkbox"/>	Test Site	<input type="checkbox"/>	Packing/Shipping/Labeling	<input type="checkbox"/>	Test Process
<input type="checkbox"/>	Wafer Bump Site	<input type="checkbox"/>	Wafer Bump Material	<input type="checkbox"/>	Wafer Bump Process
<input type="checkbox"/>	Wafer Fab Site	<input type="checkbox"/>	Wafer Fab Materials	<input type="checkbox"/>	Wafer Fab Process

PCN Details	
Description of Change:	
<p>The product datasheet(s) is being updated to change the description in device synchronization and latency specifications in order to reflect accurate operation. Information regarding the on-chip phase-locked loop is also updated to describe additional production test coverage and device capabilities.</p> <p>The following change history provides further details. These changes may be reviewed at the datasheet links provided.</p>	

Changes from Revision D (August 2012) to Revision E
Page

• Changed Power Supply Specification Table under Electrical Specification. This specification depends on the enhanced production test coverage and is specific to devices with certain date code. Refer to Clarifications for DAC3482 Power Supply and Phase-Locked Loop Specification Section for details	12
• Deleted Note (5) in Power Consumption Specification to reflect the latest DAC3482 speed specification.	12
• Changed DACCLKP/N typical clock swing specification to reflect commonly used LVPECL driver	13
• Changed DACCLKP/N typical clock swing specification to reflect commonly used LVPECL driver	13
• Changed DACCLK driver requirement to reflect actual device performance under commonly used LVPECL drivers	13
• Changed Analog Output Specification Table under Electrical Specification. This specification depends on the enhanced production test coverage and is specific to devices with certain date code. Refer to Clarifications for DAC3482 Power Supply and Phase-Locked Loop Specification Section for details	16
• Changed Digital Latency Specification for QMC to reflect the actual DAC3482 parameter	16
• Changed Digital Latency Specification for Inverse Sinc to reflect the actual DAC3482 parameter	16
• Added Phase-Locked Loop Specification Table under Electrical Specification. This specification depends on the enhanced production test coverage and is specific to devices with certain date code. Refer to Clarifications for DAC3482 Power Supply and Phase-Locked Loop Specification Section for details	17
• Changed pll_vco(6:0) to pll_vco(5:0) to reflect actual bit width in the register	40
• Changed config45, bit12:1 default value to reflect the actual default register value	45
• Changed config45, bit0 description to clarify additional DAC3482 behavior	45
• Changed syncsel_fifoout(3:0) description to clarify the FIFO read pointer reset capture method and limitation	50
• Changed information to SINGLE SYNC SOURCE MODE section to clarify the latency limitation of Single Sync Source Mode	52
• Added "the effect of bypassing the FIFO" in the Bypass Mode section to clarify the operation of FIFO, LVDS FRAME, and LVDS SYNC in FIFO Bypass Mode	53
• Changed PLL Mode section with additional operating recommendations for the DAC3482 on-chip PLL	55
• Changed information to MULTI-DEVICE OPERATION: SINGLE SYNC SOURCE MODE section to clarify the latency limitation of Single Sync Source Mode	59
• Changed Figure 64 to clarify the latency limitation of Single Sync Source Mode	60
• Changed Data Pattern Checker section with additional operating recommendations	69
• Added additional requirements for Block Parity section when byte wide input data mode is selected	72
• Changed the NCO setting description in the Example Start-up Sequence Section to reflect the example register writes	75

Device Family	Change From:	Change To:
DAC3482	SLAS748D	SLAS748E

The updated datasheet(s) can be accessed by the following link(s):

<http://www.ti.com/product/dac3482>

Reason for Change:			
To accurately reflect device characteristics and device capabilities.			
Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):			
Electrical specification performance changes as indicated above.			
Changes to product identification resulting from this PCN:			
None			
Product Affected:			
DAC3482IRKD25	DAC3482IRKDT	DAC3482IZAYR	
DAC3482IRKDR	DAC3482IZAY		

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

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