PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCN No.	IPD/15/9212
1.3 Title of PCN	L6699 (Product Line U340) : Metal mask modification
1.4 Product Category	Advanced controller
1.5 Issue date	2015-04-30

2. PCN Team	
2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Francesca Marta SANDRINI
2.1.2 Marketing Manager	Vincenzo MONTEMEZZO
2.1.3 Quality Manager	Paolo MORETTI

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Die redesign	Functional / pin layout change	Ang Mo Kio, Singapore

4. Description of change		
	Old	New
4.1 Description	U340BC6	U340BD6
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	No impact.	

5. Reason / motivation for change	
5.1 Motivation	To enlarge the pin Line functionality with dv/dt lower than 100V/second
5.2 Customer Benefit	QUALITY IMPROVEMENT

6. Marking of parts / traceability of change	
6.1 Description	By a new Finished Goods code. L6699D-6/ L6699DTR-6/

7. Timing / schedule	
7.1 Date of qualification results	2015-04-20
7.2 Intended start of delivery	2015-10-05
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation			
8.1 Description	U340 Reliability Report.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2015-04-30

9. Attachments (additional documentations)

9212PpPrdtLst.pdf
U340 detail_descr_template.pdf
U340 Reliability Report.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	L6699D	
	L6699DTR	

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Public Products List

PCN Title : L6699 (Product Line U340) : Metal mask modification

PCN Reference : IPD/15/9212

PCN Created on : 20-Apr-2015

Subject : Public Product List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

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L6699 (Product Line U340) : Metal mask modification

WHAT is the change?

The Internal Supply Rail of the Line Comparator has been changed. See the following pages.

WHY?

The change was made to solve the following issue:

A signal applied to the Line pin with a slope lower than 100V/second could cause the device stops switching even though the voltage at Line pin is higher than its threshold (1.25V).

WHEN will this change occur?

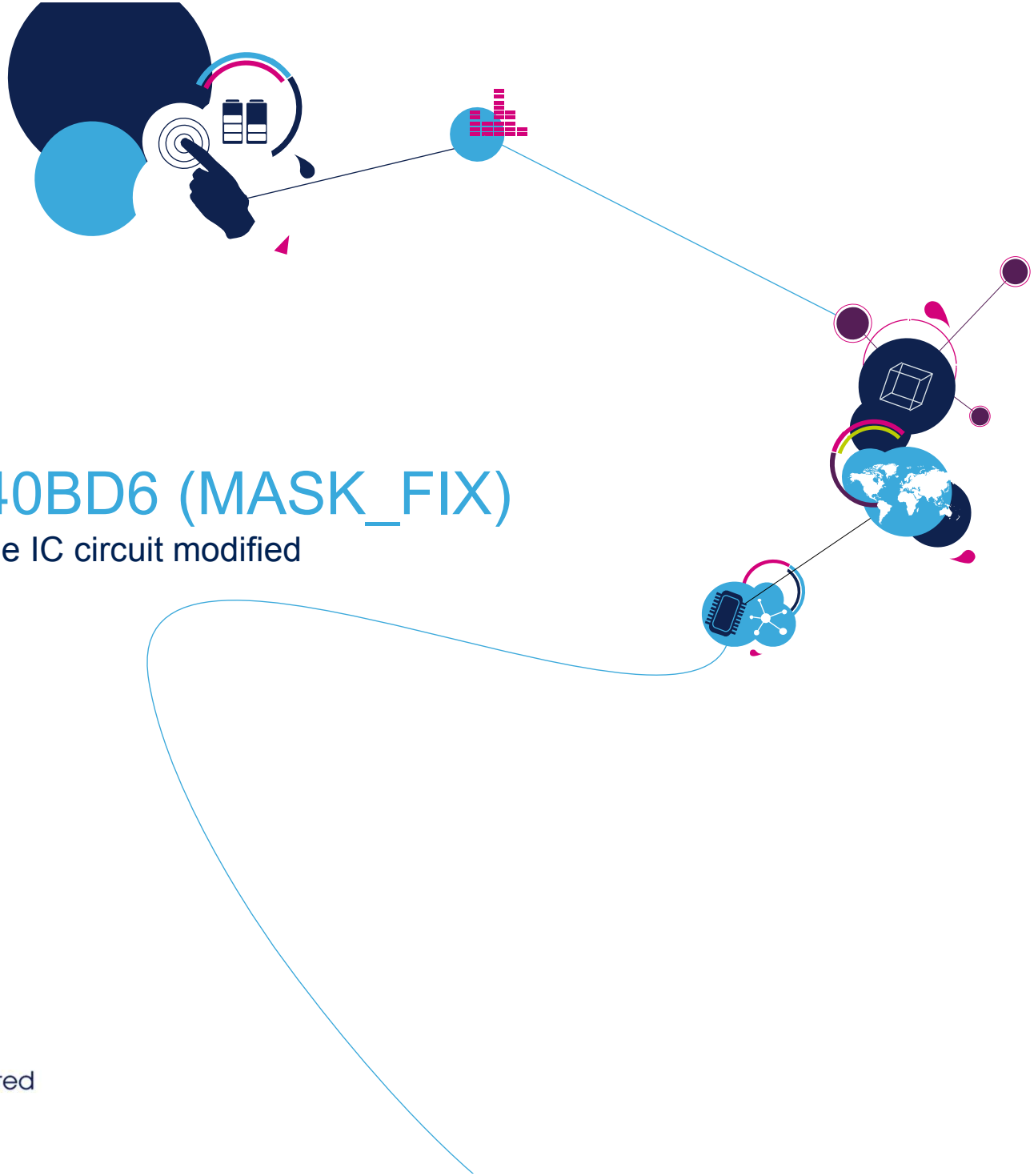
Tentatively at the beginning of Q4 2015. However the production of the new product will be based on material availability and customers' orders. Phase-out and phase-in will be done accordingly.

HOW will the change be qualified?

See the attached Report for the product reliability. Functional effectiveness has been confirmed by the application trial results.

IMPACTS of the Change

Form: No impact
Fit: No impact
Function: yes, improved.

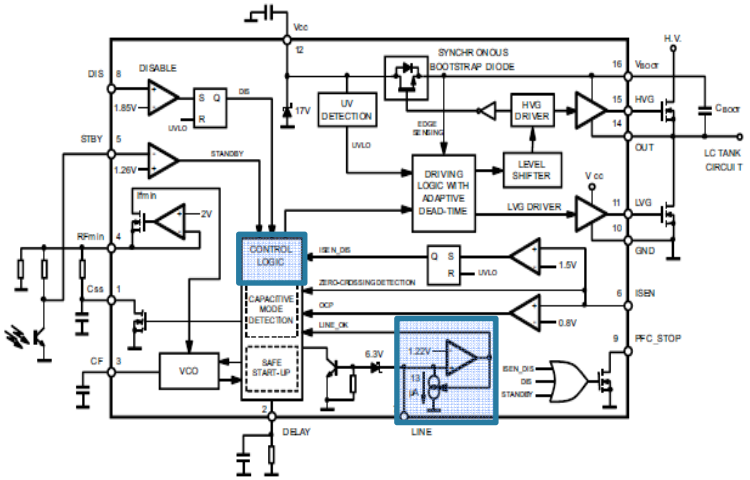


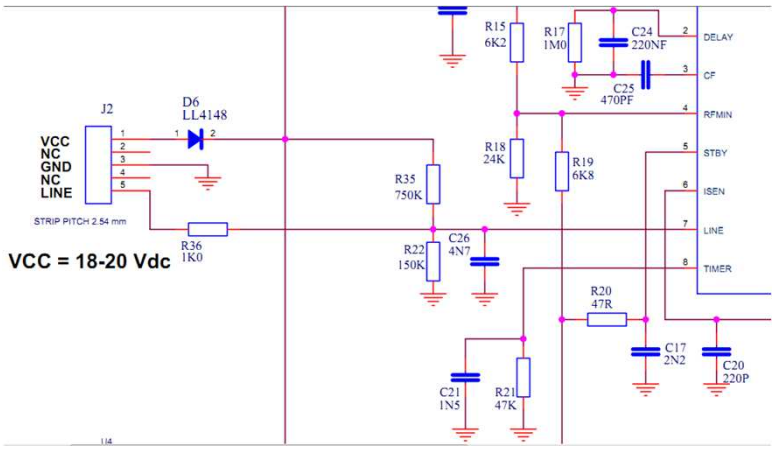
L6699D U340BD6 (MASK_FIX)

Summary Report of the IC circuit modified

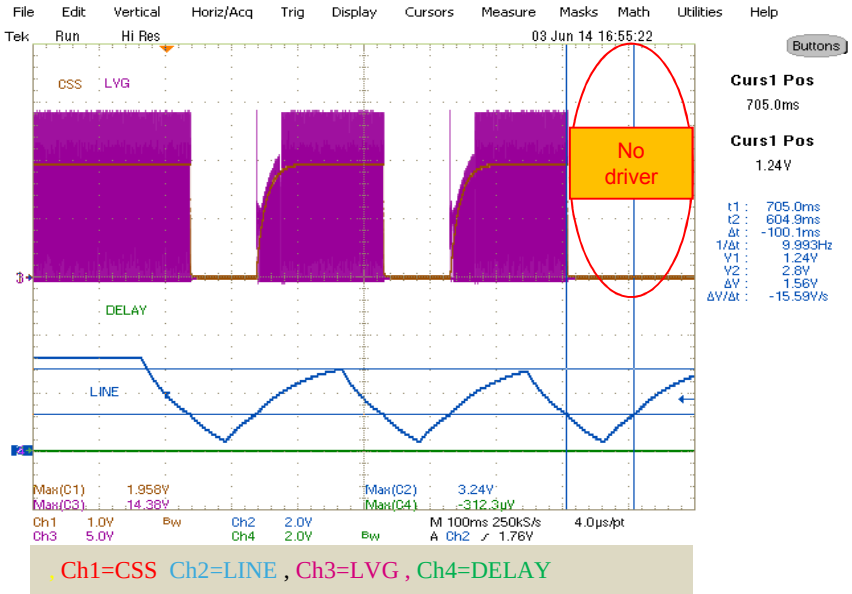
life.augmented

Partial schematic from application





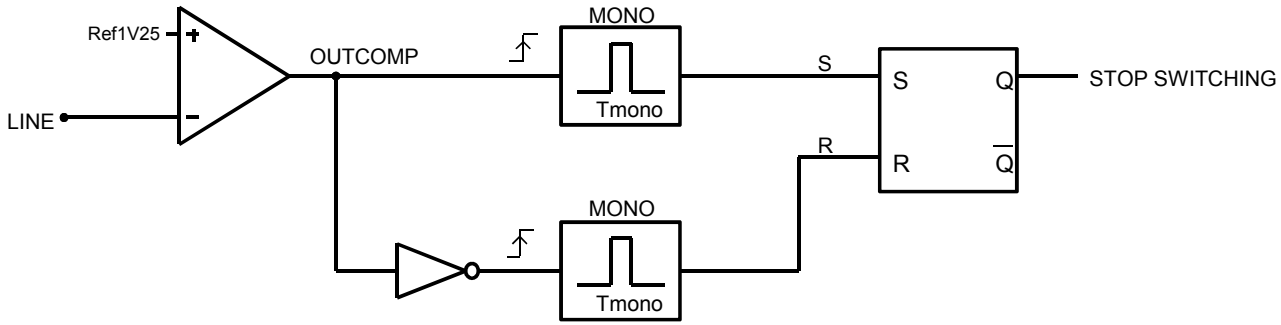
- When LINE pin of L6699 is used as IC disable with a dvt/dt <100V/s, sometimes we can find that power did not turn on for Vline higher than 1.25V.

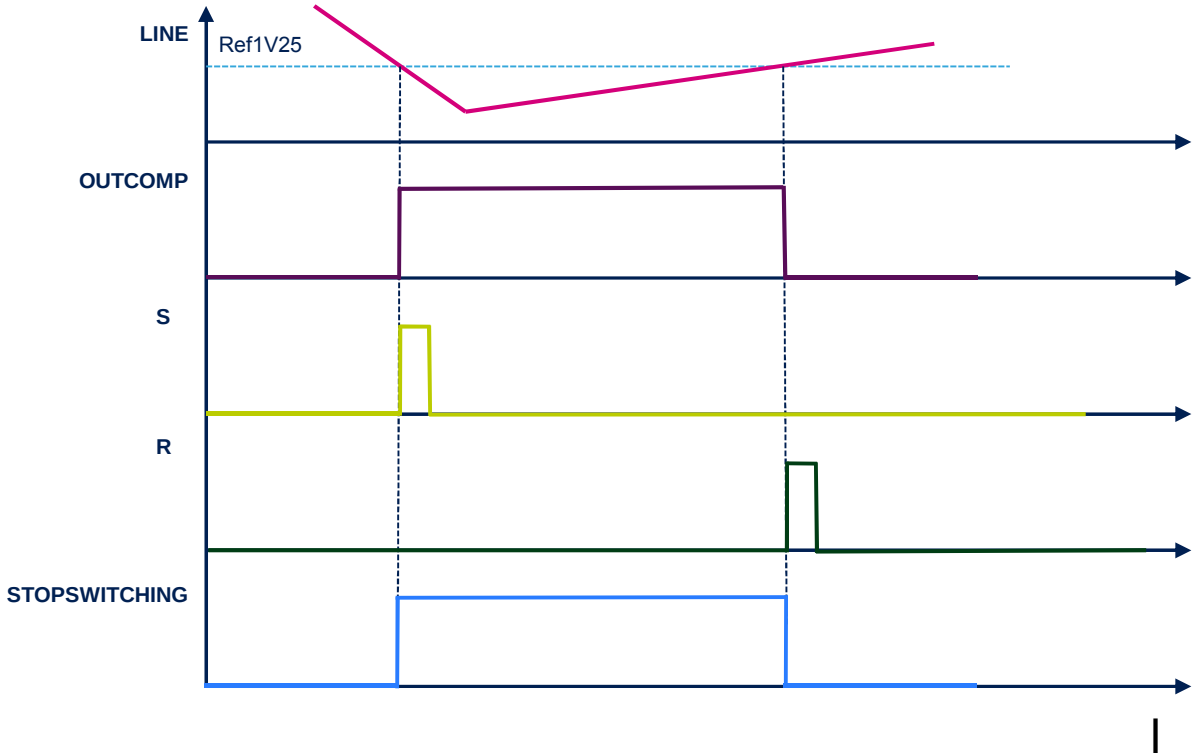


. Ch1=CSS Ch2=LINE , Ch3=LVG , Ch4=DELAY

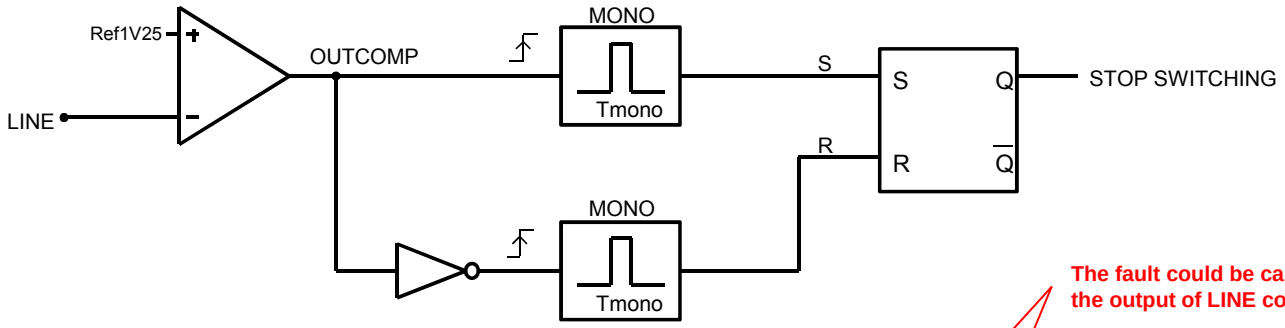
ST confidential

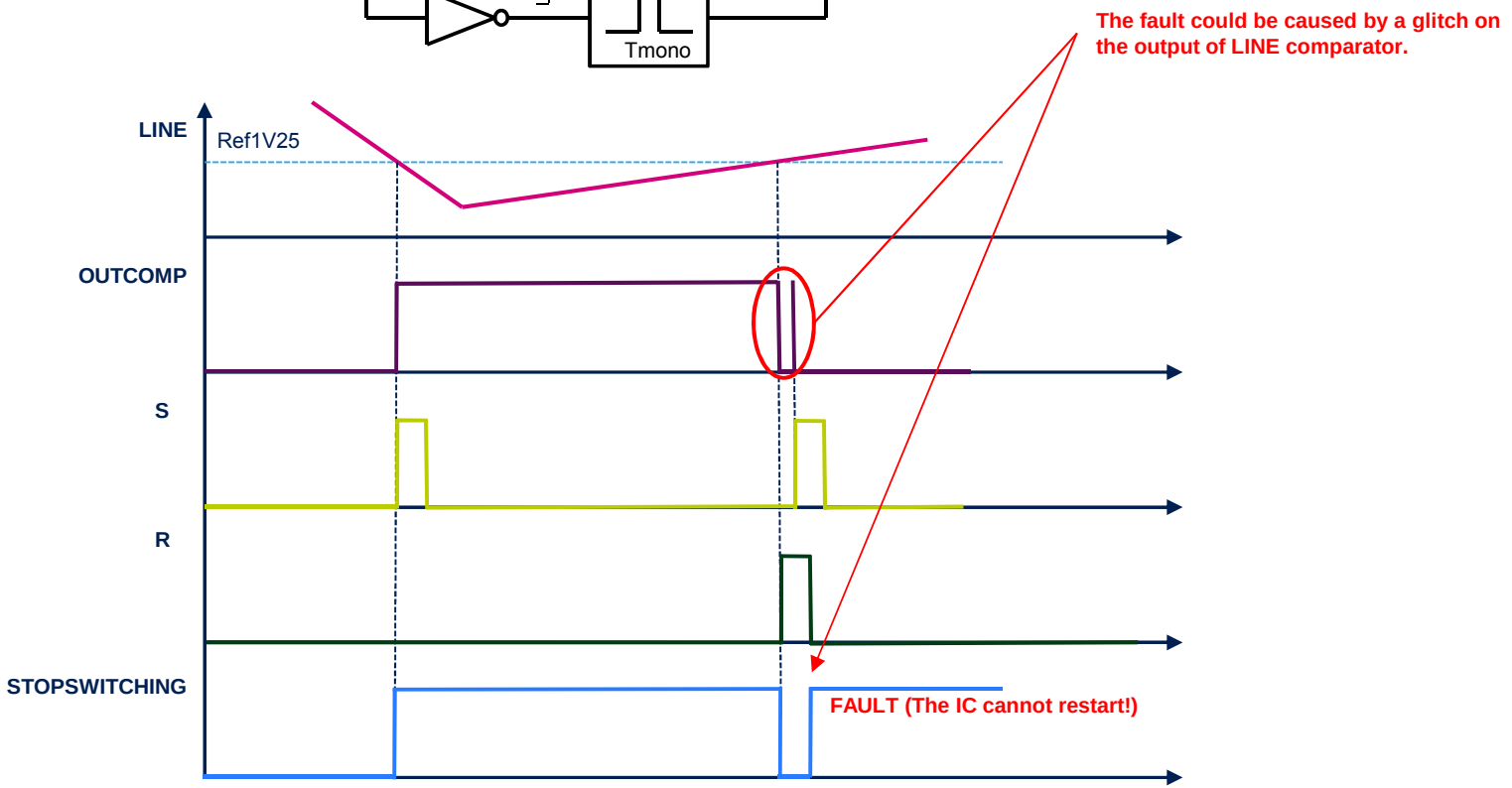
Correct stop and restart switching by LINE





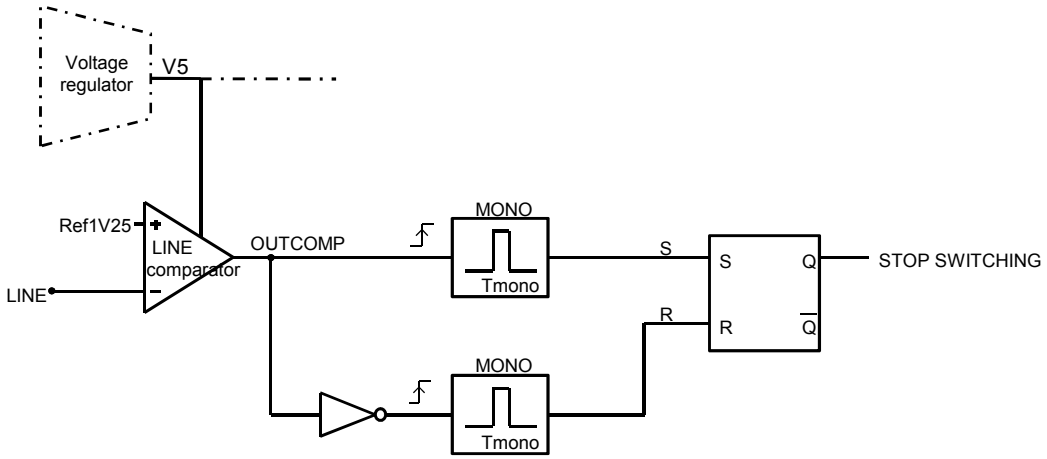
Fault on restart switching by LINE

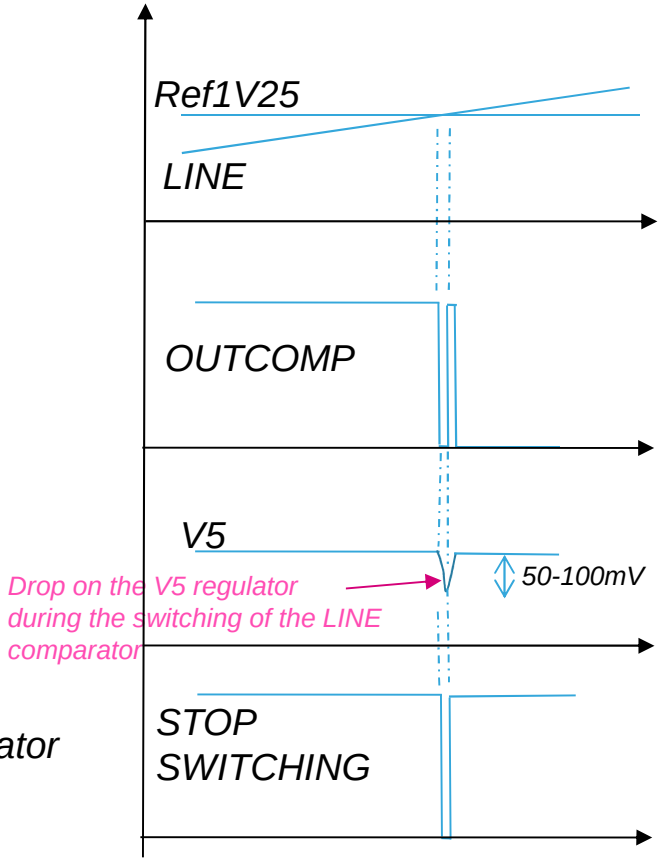




life.augmented

Root-cause of the glitch



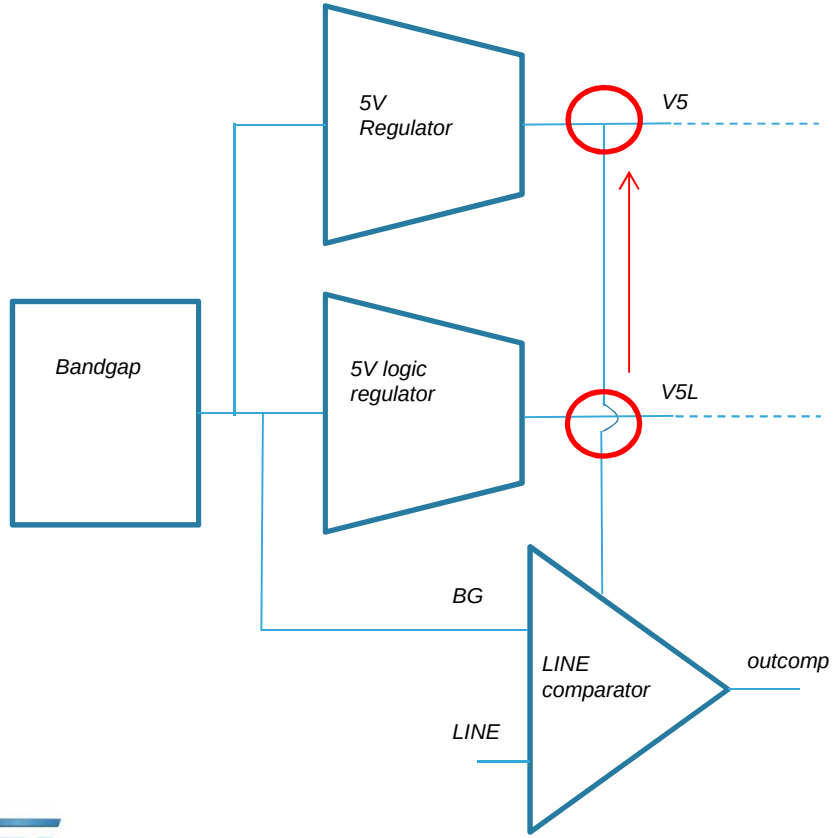


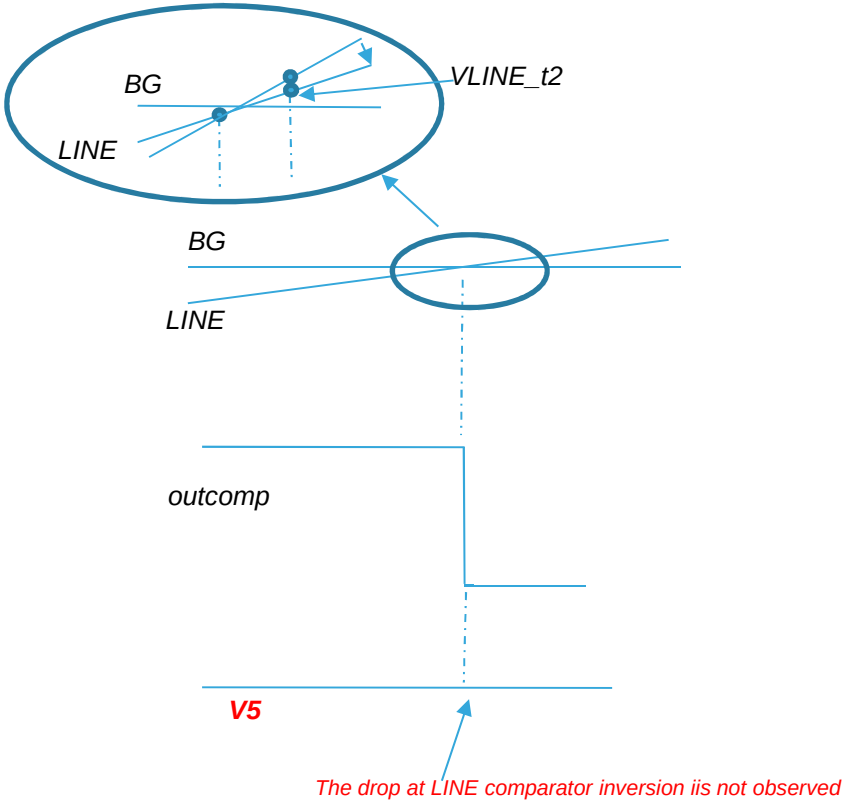
The glitch on the output of the LINE comparator occurs with low slopes of the LINE signal and it is due to the drop of the V5 regulator during the commutation.

The occurrence of the glitch depends on the slope of the LINE signal. (Below a slope limit the glitch appears always due to V5 drop and because the LINE voltage is closer to the Ref1V25 during the commutation of the comparator.)

Implemented Fix

- To avoid the problem the Line Comparator supply has been replaced by an internal 5V regulator with a stronger current capability.





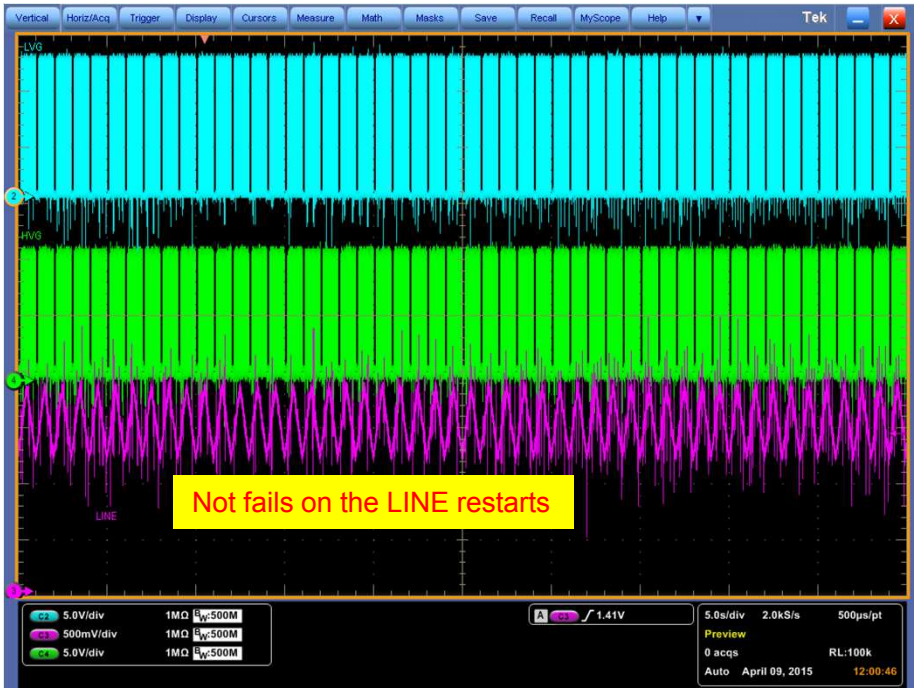
IC Design Validation: *U340BD6 vs U340BC6*
Plastic sample – Demo Board

U340BC6 Old Silicon version

CH1: Idrain HVG	CH2:LVG	CH3	CH4:HVG

- U340BC6. With dV_{LINE}/dt <100V/s, sometimes we can find that power did not turn on during the cross of LINE threshold of 1.25V.

U340BD6 New Silicon version



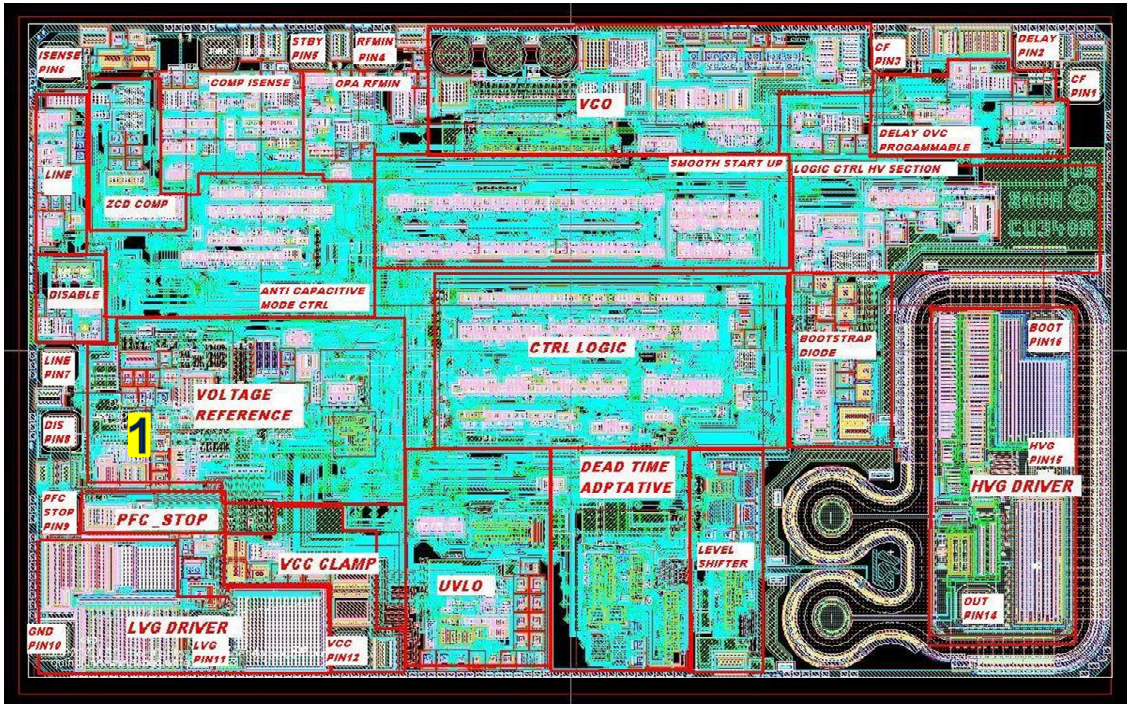
CH1: Idrain HVG	CH2:LVG	CH3	CH4:HVG

- U340BD6. With dV_{LINE}/dt <100V/s, the IC always restarts when the threshold of LINE (1.25V) is crossed.

From U340BC6 to U340BD6

1. U340BD BCDOFFLINE Masks fixed
2. Mask changed: poly2,contact,metal1
3. No spec changed/No critical metal path VCC, GND or ESD protection

FUNTIONS / BUGS	U340BC6	U340BD6
1) The IC does not re-enable when the voltage LINE threshold is crossed with dV/dt very slow.	Noise of the output logic LINE, supplied by V5L (internal voltage regulator).	Logic LINE comparator is supplied by a different internal voltage regulator with a current capability higher than V5L to increase the noise immunity.



Reliability Report

General Information	
Product Line	*U340*
Product Description	*Enhanced high-voltage resonant controller*
Product division	*I&PC*
Package	*SO16N*
Silicon process technology	*BCD OFF LINE*

Locations	
Wafer fab location	*ANG MO KIO*
Assembly plant location	*AMKOR ATP1 PHILIPPINES*
Reliability assessment	*Pass*

DOCUMENT HISTORY

Version	Date	Pages	Author	Comment
1.0	17-April-2015	12	G. Capodici	Original document

Reviewed by

Alceo Paratore

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	: Stress test qualification for integrated circuits
8161393A	: General Specification For Product Development

2 RELIABILITY EVALUATION OVERVIEW

2.1 Objectives

This report contains the reliability activity done on the U340 device diffused in ANG MO KIO and assembled in SO16N in AMKOR ATP1 PHILIPPINES.

According to Reliability Qualification Plan, below is the list of the trials performed:

Die Oriented Tests

- High Temperature Operating Life test
- High Temperature Reverse Bias
- Temperature Humidity Bias

Package Oriented Tests

- Preconditioning

Electrical Characterization

- ESD resistance test
- LATCH-UP resistance test

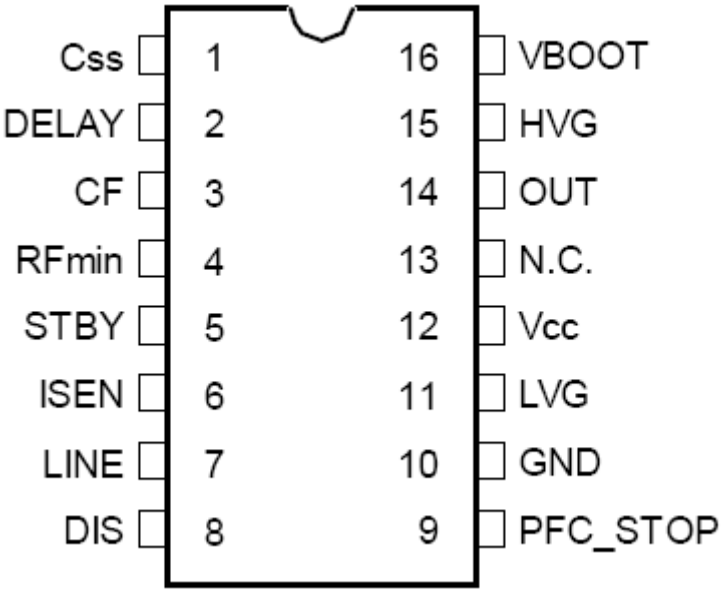
2.2 Conclusion

Taking in account the results of the trials performed **the U340 diffused in ANG MO KIO and assembled in SO16N in AMKOR ATP1 PHILIPPINES can be qualified from reliability viewpoint.**

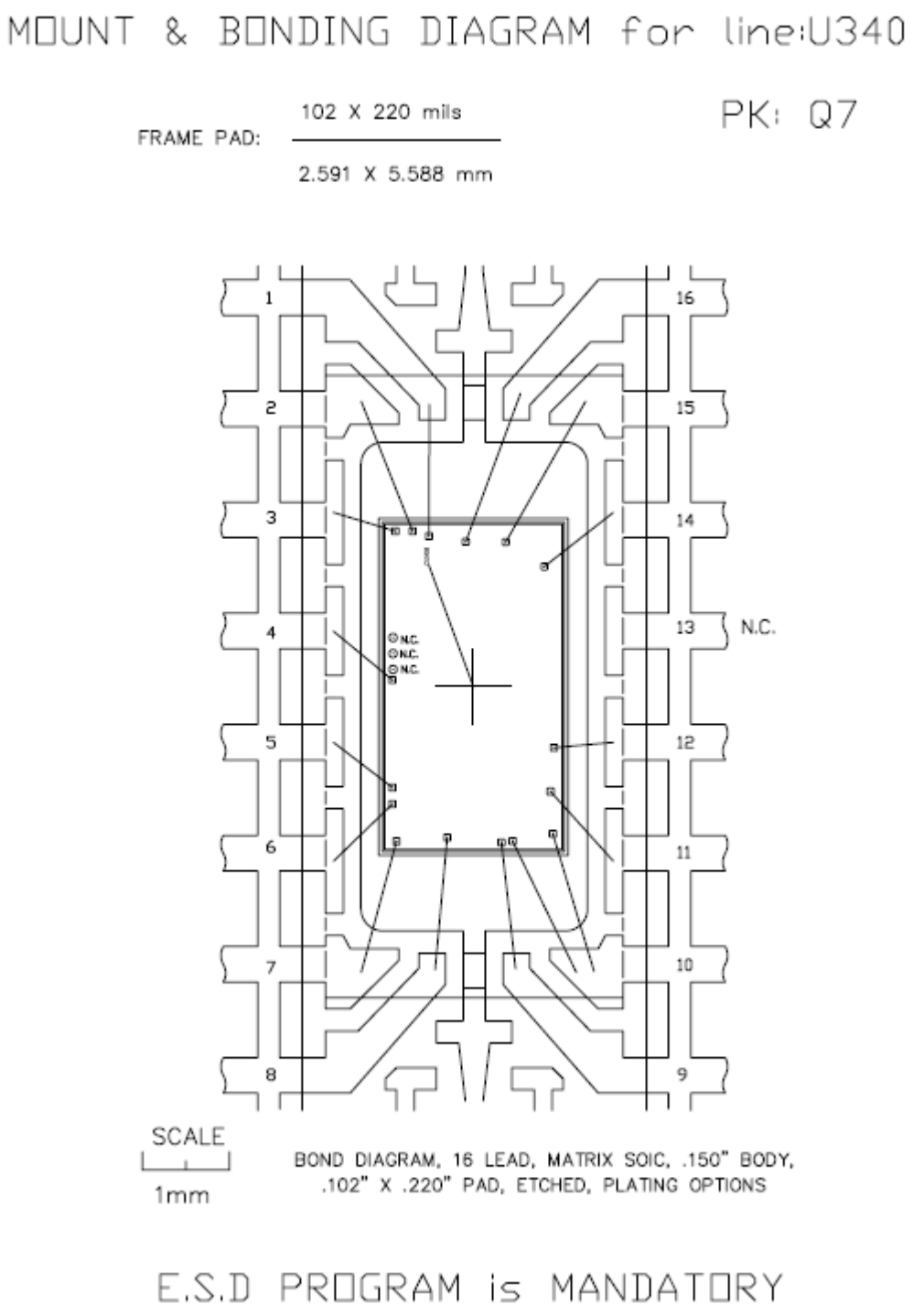
3 DEVICE CHARACTERISTICS

3.1 Device description

3.1.1 Pin connection



3.1.2 Bonding diagram

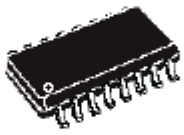


3.1.3 Package outline/Mechanical data

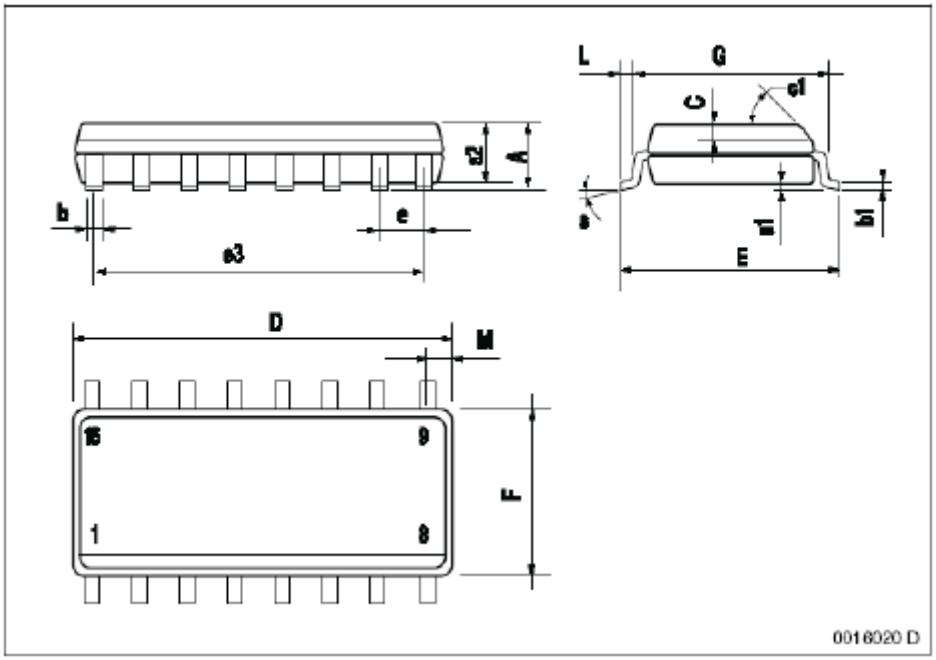
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.009
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1			45°	(typ.)		
D(1)	9.8		10	0.386		0.394
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F(1)	3.8		4.0	0.150		0.157
G	4.60		5.30	0.181		0.208
L	0.4		1.27	0.150		0.050
M			0.62			0.024
S	8 ° (max.)					

(1) "D" and "F" do not include mold flash or protrusions - Mold flash or protrusions shall not exceed 0.15mm (.006inc.)

OUTLINE AND MECHANICAL DATA



SO16 (Narrow)



4 TRACEABILITY

Wafer fab information	
Wafer fab manufacturing location	*ANG MO KIO*
Wafer diameter	*6 inches*
Wafer thickness	*375µm*
Silicon process technology	*BCD OFF LINE*
Die finishing back side	*Cr/Ni*
Die size	*3870x2190µm*
Bond pad metallization layers	*AlSiCu*
Passivation	*SiN*
Metal levels	*1*

Assembly Information	
Assembly plant location	*AMKOR ATP1 PHILIPPINES*
Package description	*SO16N*
Molding compound	*SUMITOMO G600*
Wires bonding materials/diameters	*Au / 1mils*
Die attach material	*ABLESTICK 8290*
Lead solder material	*Sn*

5 TESTS RESULTS SUMMARY

5.1 Test plan and results summary

Test	Test short description					
	Method	Conditions	Sample/Lots	Number of lots	Duration	Results Fail/SS
PC	Pre-Conditioning: Moisture sensitivity level 3					
		192h 30°C/60%RH- 3 reflow PBT 260°C	**157**	1	**-**	**0/157**
HTRB	High Temperature Reverse Bias - Positive					
		Conditions : Vs=600V, VCC=16V Tj=150 °C;	**40**	1	**1000h**	**0/40**
HTOL	High Temperature Operating Life Test					
	PC before	**Vs=580V, VCC=16V, Tj=150 °C;**	**77**	1	**1000h**	**0/77**
THB	Temperature Humidity Bias					
	PC before	**Vs=100V, VCC=16V, Ta=85°C / 85%R.H.;**	**40**	1	**1000h**	**0/40**
ESD	Electro Static Discharge					
	Human Body Model	**+/- 2KV**	**3**	1	**-**	**0/3**
	Machine Model	**+/- 100V**	**3**	1	**-**	**0/3**
	Charge Device Model	**+/- 750V**	**3**	1	**-**	**0/3**
LU	Latch-Up					
	Over-voltage and Current Injection (Jedec78) performed at 85°C Class 2B		**3**	1	**-**	**0/3**

All above trials performed on BA6 revision.

5.2 Die oriented tests

5.2.1 High Temperature Operating Life Test

This test is performed like application conditions in order to check electromigration phenomena, gate oxide weakness and other design/manufacturing defects put in evidence by internal power dissipation.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Check @ 168 and 500hrs @ Ta=25°C
- Final Testing @ 1000hrs @ Ta=25°C

5.2.2 High Temperature Reverse Bias

This test is performed to evaluate die problems related with chip stability, layout structure, surface contamination and oxide faults.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Check @ 168 and 500hrs @ Ta=25°C
- Final Testing @ 1000hrs @ Ta=25°C

5.2.3 Temperature Humidity Bias

The test is addressed to put in evidence problems of the die-package compatibility related to phenomena activated in wet conditions such as electro-chemical corrosion.
The device is stressed in static configuration approaching some field status like power down. Temperature, Humidity and Bias are applied to the device in the following environmental conditions => Ta=85°C / RH=85%.
Input pins to Low / High Voltage (alternate) to maximize voltage contrast.
Test Duration 1000 h.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Check @ 168 and 500hrs @ Ta=25°C
- Final Testing @ 1000hrs @ Ta=25°C

5.3 Package oriented tests

5.3.1 Pre-Conditioning

The device is submitted to a typical temperature profile used for surface mounting,
after a controlled moisture absorption.
The scope is to verify that the surface mounting stress does not impact on the subsequent reliability performance.
The typical failure modes are "pop corn" effect and delamination.

5.4 Electrical Characterization Tests

5.4.1 Latch-up

This test is intended to verify latch-up sensitivity for new product or new process qualification.
Method applied: Ip = +/- 100mA for each pin according to 0018695 S.T. spec. (referring to Jedec Std-78).
The flow chart is the following:

- Initial testing @ Ta=25°C
- Latch-up trail performed @ Ta=25°C
- Final Testing @ Ta=25°C

Condition	NEG. INJECTION	POS. INJECTION	OVERVOLTAGE
IN low: 0V	-30mA	Inom+100mA	VCC= 17V BOOT= 17V
IN high: 0.7V	-30mA	Inom+100mA	VCC= 17V BOOT= 17V

5.4.2 E.S.D.

This test is performed to verify adequate pin protection to electrostatic discharges.
The flow chart is the following:

- Initial testing @ Ta=25°C
- ESD discharging @ Ta=25°C
- Final Testing @ Ta=25°C

TEST CONDITIONS:

- **Human Body Model** — JEDEC STANDARD JESD22-A114
CDF-AEC-Q100-002
- **Machine Model** — JEDEC STANDARD EIA/JESD-A115
CDF-AEC-Q100-003
- **Charge Device Model** — ANSI/ESD STM 5.3.1 ESDA
CDF-AEC-Q100-011