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FQU4N50TU_WS

N-Channel QFET® MOSFET

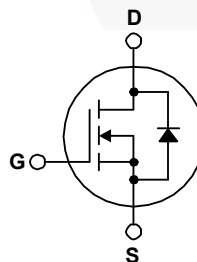
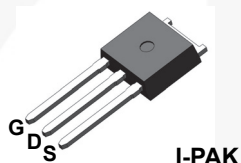
500 V, 2.6 A, 2.7 Ω

Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 2.6 A, 500 V, $R_{DS(on)} = 2.7 \Omega$ (Max.) @ $V_{GS} = 10 V$, $I_D = 1.3 A$
- Low Gate Charge (Typ. 10 nC)
- Low Crss (Typ. 6.0 pF)
- 100% Avalanche Tested



Absolute Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted.

Symbol	Parameter	FQU4N50TU_WS	Unit
V_{DSS}	Drain-Source Voltage	500	V
I_D	Drain Current - Continuous ($T_C = 25^\circ C$)	2.6	A
	- Continuous ($T_C = 100^\circ C$)	1.64	A
I_{DM}	Drain Current - Pulsed (Note 1)	10.4	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	260	mJ
I_{AR}	Avalanche Current (Note 1)	2.6	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	4.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
P_D	Power Dissipation ($T_A = 25^\circ C$) *	2.5	W
	Power Dissipation ($T_C = 25^\circ C$)	45	W
	- Derate above $25^\circ C$	0.36	W/ $^\circ C$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ C$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ C$

Thermal Characteristics

Symbol	Parameter	FQU4N50TU_WS	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	2.78	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	110	
	Thermal Resistance, Junction to Ambient (*1 in ² Pad of 2-oz Copper), Max.	50	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQU4N50TU_WS	FQU4N50S	IPAK	Tube	N/A	N/A	75 units

Electrical Characteristics T_c = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	500	--	--	V
ΔBV _{DSS} / ΔT	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	--	0.38	--	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 500 V, V _{GS} = 0 V	--	--	1	μA
		V _{DS} = 400 V, T _C = 125°C	--	--	10	μA
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 30 V, V _{DS} = 0 V	--	--	100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -30 V, V _{DS} = 0 V	--	--	-100	nA

On Characteristics

V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	3.0	--	5.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 1.3 A	--	2.0	2.7	Ω
g _{FS}	Forward Transconductance	V _{DS} = 50 V, I _D = 1.3 A	--	2.6	--	S

Dynamic Characteristics

C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz	--	350	460	pF
C _{oss}	Output Capacitance		--	55	70	pF
C _{rss}	Reverse Transfer Capacitance		--	6	8	pF

Switching Characteristics

t _{d(on)}	Turn-On Delay Time	V _{DD} = 250 V, I _D = 3.4 A, R _G = 25 Ω	--	12	30	ns	
t _r	Turn-On Rise Time		--	45	100	ns	
t _{d(off)}	Turn-Off Delay Time		--	20	50	ns	
t _f	Turn-Off Fall Time		(Note 4)	--	30	70	ns
Q _g	Total Gate Charge	V _{DS} = 400 V, I _D = 3.4 A, V _{GS} = 10 V	--	10	13	nC	
Q _{gs}	Gate-Source Charge		(Note 4)	--	2.5	--	nC
Q _{gd}	Gate-Drain Charge		(Note 4)	--	4.7	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I _S	Maximum Continuous Drain-Source Diode Forward Current	--	--	2.6	A	
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	10.4	A	
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 2.6 A	--	--	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 3.4 A,	--	210	--	ns
Q _{rr}	Reverse Recovery Charge	dI _F / dt = 100 A/μs	--	1.15	--	μC

Notes:

1. Repetitive rating : pulse-width limited by maximum junction temperature.
2. L = 68 mH, I_{AS} = 2.6 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 3.4 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.
4. Essentially independent of operating temperature.

Typical Characteristics

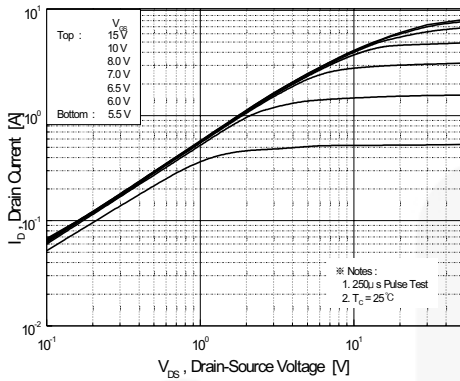


Figure 1. On-Region Characteristics

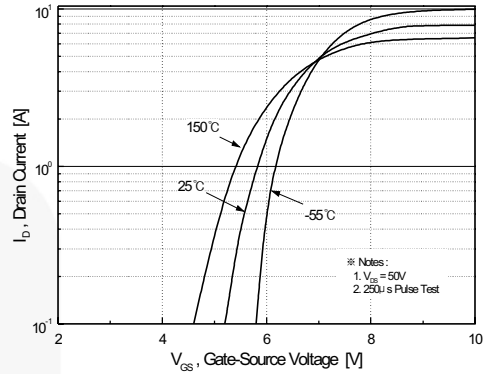


Figure 2. Transfer Characteristics

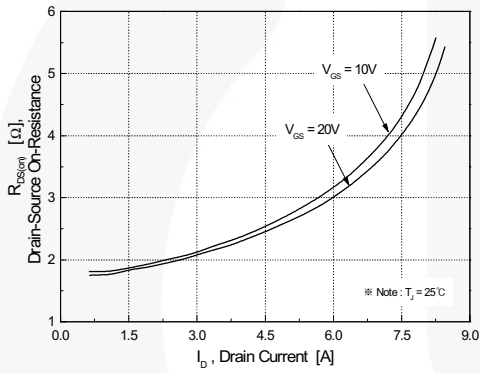


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

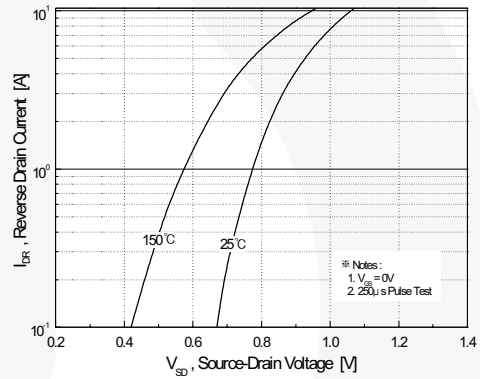


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

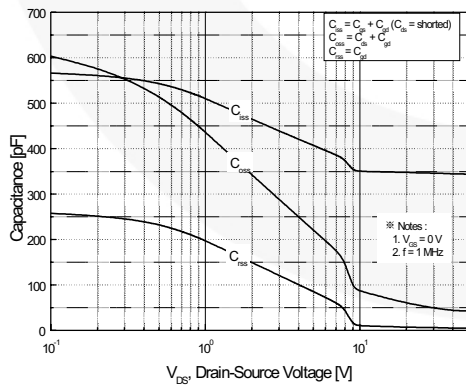


Figure 5. Capacitance Characteristics

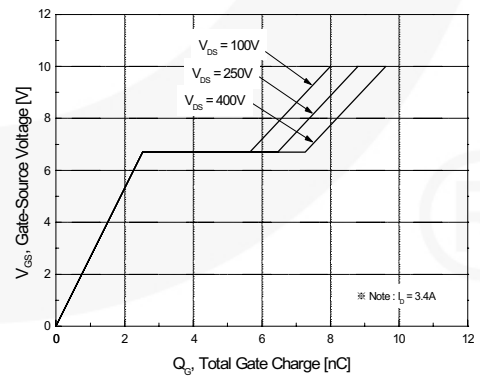


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

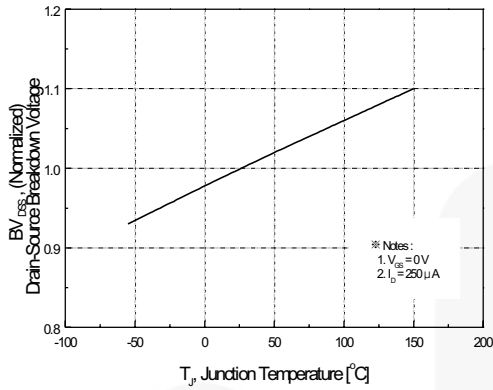


Figure 7. Breakdown Voltage Variation vs. Temperature

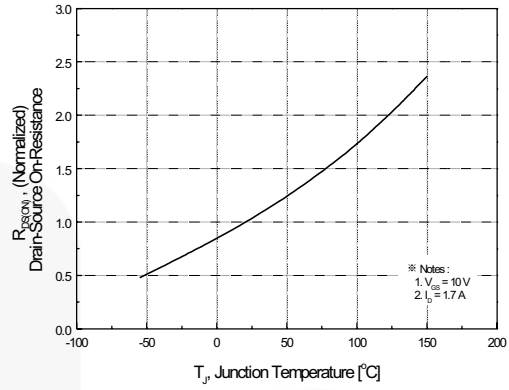


Figure 8. On-Resistance Variation vs. Temperature

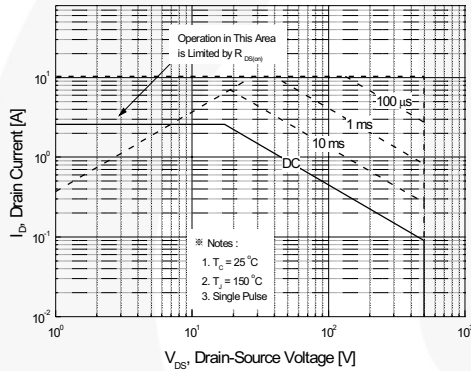


Figure 9. Maximum Safe Operating Area

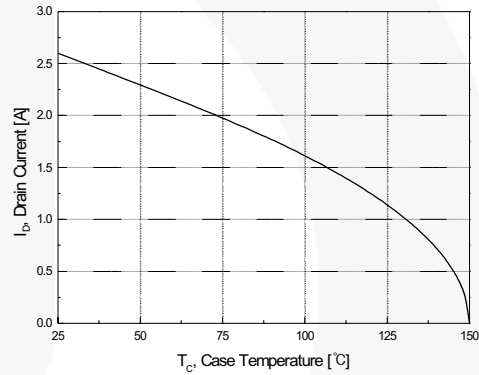


Figure 10. Maximum Drain Current vs. Case Temperature

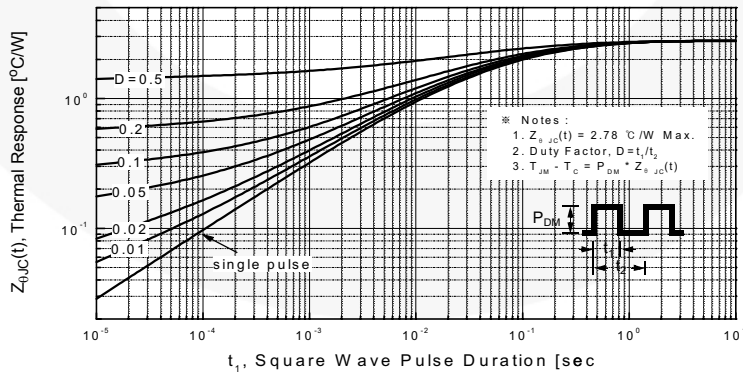


Figure 11. Transient Thermal Response Curve



Figure 12. Gate Charge Test Circuit & Waveform



Figure 13. Resistive Switching Test Circuit & Waveforms

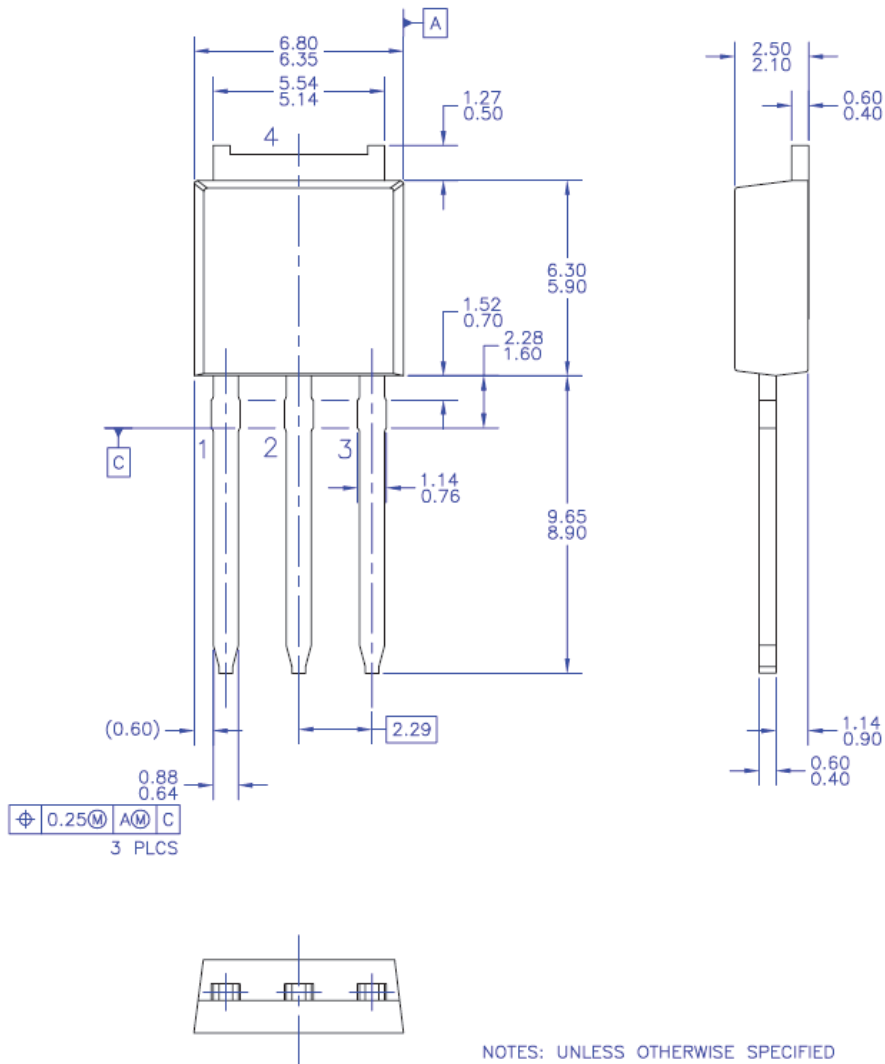


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

- A) ALL DIMENSIONS ARE IN MILLIMETERS.
- B) THIS PACKAGE CONFORMS TO JEDEC, TO-251, ISSUE C, VARIATION AA, DATED SEP 1988.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

Figure 16. TO-251 (I-PAK), Molded, 3-Lead, Option AA

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