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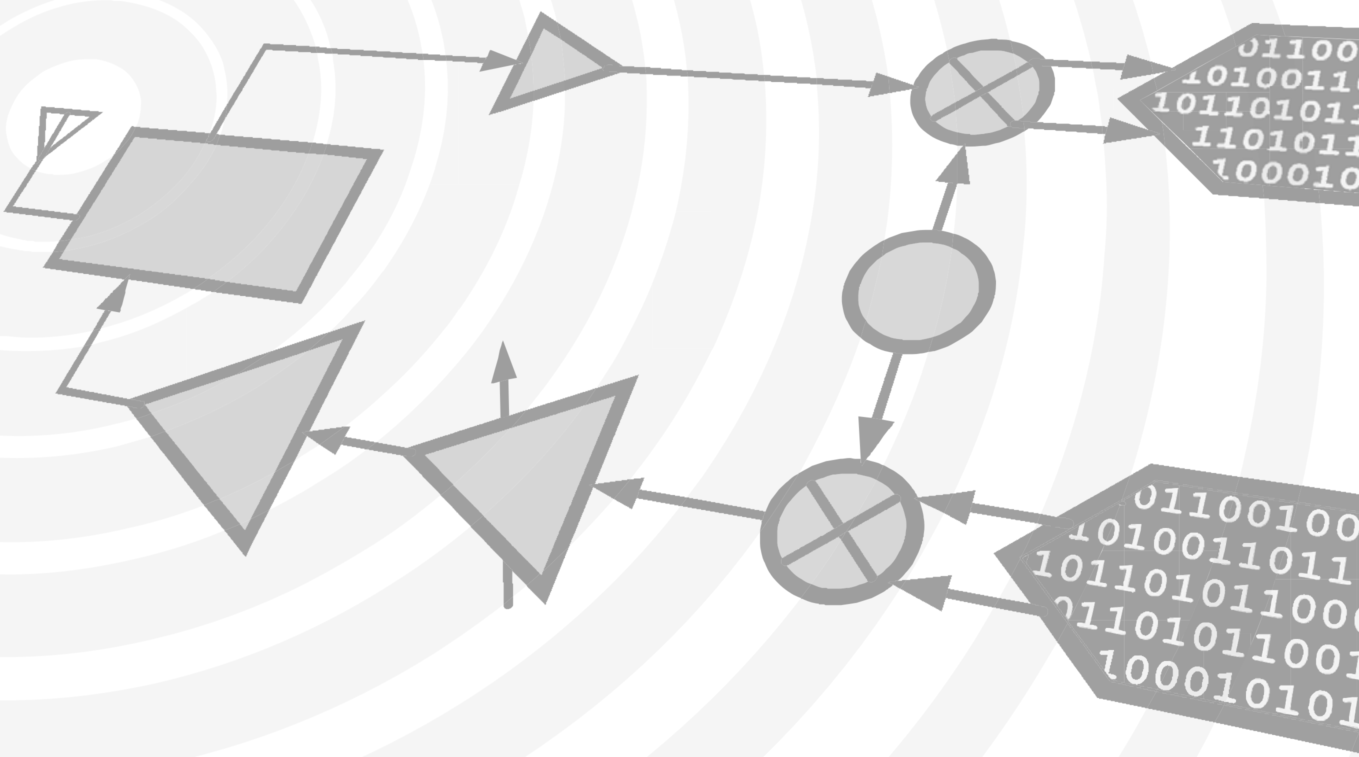
NO CONTENT ON THE ATTACHED DOCUMENT HAS CHANGED



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RMS POWER DETECTOR SINGLE-ENDED, DC - 3.9 GHz

Typical Applications

The HMC1020LP4E is ideal for:

- Log –> Root-Mean-Square (RMS) Conversion
- Tx/Rx Signal Strength Indication (TSSI/RSSI)
- RF Power Amplifier Efficiency Control
- Receiver Automatic Gain Control
- Transmitter Power Control

Features

Broadband Single-Ended RF Input

±1 dB Detection Accuracy to 3.9 GHz

Input Dynamic Range: -65 dBm to +7 dBm

RF Signal Wave Shape & Crest Factor Independent

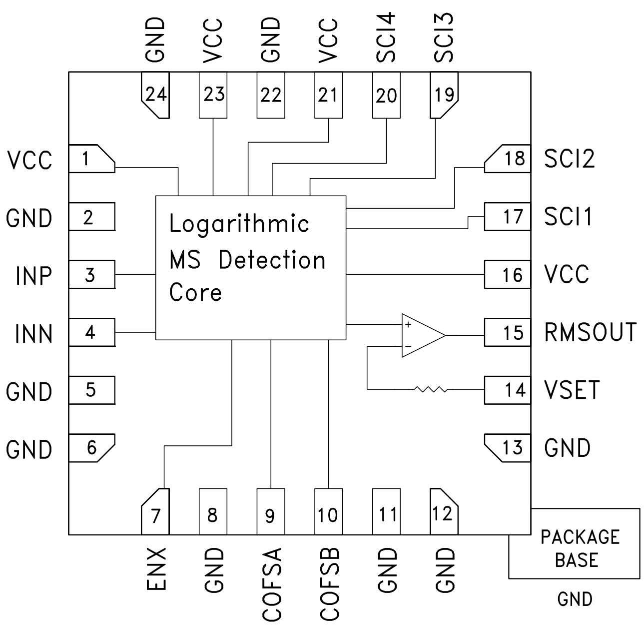
Digitally Programmable Integration Bandwidth

Excellent Temperature Stability

Power-Down Mode

24 Lead 4x4mm SMT Package: 16mm²

Functional Diagram



General Descriptions

The HMC1020LP4E Power Detector is designed for RF power measurement and control applications for frequencies up to 3.9 GHz. The detector provides an accurate RMS representation of any broadband, single-ended RF/IF input signal. The output is a temperature compensated, monotonic representation of real signal power, measured with an input sensing range of 72 dB.

The HMC1020LP4E is ideally suited to those wide bandwidth, wide dynamic range applications requiring repeatable measurement of real signal power, especially where RF/IF wave shape and/or crest factor change with time.

The integration bandwidth of the HMC1020LP4E is digitally programmable with the use of input pins SCI1-4 over a range of more than 3 decades. This allows the user to dynamically set the operation bandwidth and also permits the detection of different types of modulations on the same platform.

HMC1020LP4E features an internal op-amp at the output stage, which provides for slope / intercept adjustments and enables controller application.

Electrical Specifications I

T_A = +25 °C, Vcc = 5V, Sci4 = Sci1 = 0V, Sci3 = Sci2 = 5V, Unless Otherwise Noted

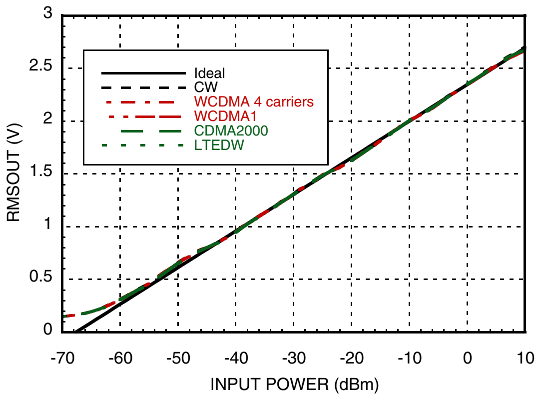
Parameter	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Units
Dynamic Range (±1dB Error) [1]								
Input Frequency	100	900	1900	2200	2700	3500	3900	MHz
Single Ended Input Configuration	72	72	71	70	66	58	53	dB
Deviation vs Temperature: (Over full temperature range -40 °C to 85 °C). Deviation is measured from reference, which is the same WCDMA input at 25 °C.						1		dB
[1] With WCDMA 4 Carrier (TMI1-64 DPCH)								

Electrical Specifications II

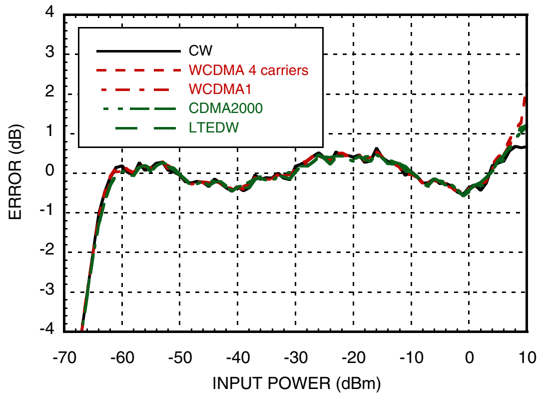
T_A = +25 °C, Vcc = 5V, Sci4 = Sci1 = 0V, Sci3 = Sci2 = 5V, Unless Otherwise Noted

Parameter	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Units
Input Frequency	100	900	1900	2200	2700	3500	3900	MHz
Modulation Deviation (Output deviation from reference, which is measured with CW input at equivalent input signal power)								
WCDMA 4 Carrier (TM1-64 DPCH) at +25 °C	0.1	0.1	0.1	0.1	0.1	0.1	0.1	dB
WCDMA 4 Carrier (TM1-64 DPCH) at +85 °C	0.1	0.1	0.1	0.1	0.1	0.1	0.1	dB
WCDMA 4 Carrier (TM1-64 DPCH) at -40 °C	0.1	0.1	0.1	0.1	0.1	0.1	0.1	dB
Logarithmic Slope and Intercept [1]								
Logarithmic Slope	35.0	35.2	36.0	36.6	37.9	41.5	44.4	mV/dB
Logarithmic Intercept	-68.2	-67.9	-66.5	-65.6	-63.6	-58.7	-55.3	dBm
Max. Input Power at ±1dB Error	7	7	7	7	5	2	0	dBm
Min. Input Power at ±1dB Error	-65	-65	-64	-63	-61	-56	-53	dBm
[1] With WCDMA 4 Carrier (TM1-64 DPCH)								

RMSOUT vs. Pin with Different Modulations @ 1900 MHz [1]



RMSOUT Error vs. Pin with Different Modulations @ 1900 MHz [1]



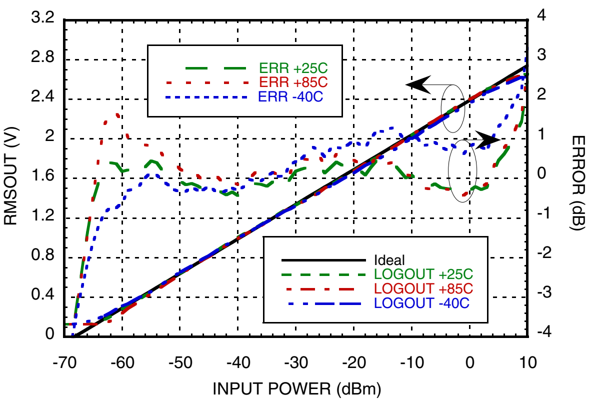
[1] Data was taken at Sci4=Sci1=0V, Sci3=Sci2=5V, shortest integration time is for SCI=0000, allowed longest integration time is for SCI=1100

Electrical Specifications III

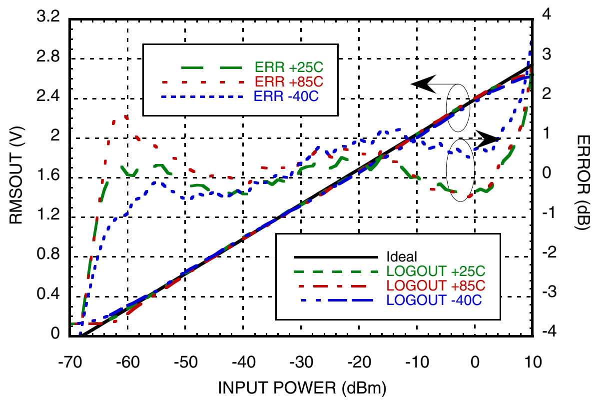
T_A = +25 °C, Vcc = 5V, Sci4 = Sci1 = 0V, Sci3 = Sci2 = 5V, Unless Otherwise Noted

Parameter	Conditions	Min	Typ.	Max	Units
Single-Ended Input Configuration					
Input Network Return Loss	up to 3.9 GHz		> 15		dB
Input Resistance between INP and INN	Between pins 3 and 4		100		Ω
Input Voltage Range	AC coupled peak voltage at INP			0.85	V
RMSOUT Output					
Output Voltage Range			0.13 to 2.7		V
Source/Sink Current Compliance	RMSOUT held at VCC/2		8 / -0.55		mA
Output Slew Rate (rise / fall)	Sci4=Sci3=Sci2=Sci1=0V, Cofs=1nF		24 / 1.9		10^6 V/s
VSET Input (Negative Feedback Terminal)					
Input Voltage Range	For control applications with nominal slope/intercept settings		0.13 to 2.7		V
Input Resistance			5		MΩ
SCI1-4 Inputs, ENX Logic Input (Power Down Control)					
Input High Voltage		0.7xVCC			V
Input Low Voltage				0.3xVCC	V
Input High Current				1	µA
Input Low Current				1	µA
Input Capacitance			0.5		pf
Power Supply					
Supply Voltage		4.5	5	5.5	V
Supply Current with no input power			55		mA
Supply Current with Pin = -20dBm			58		mA
Standby Mode Supply Current			5		mA

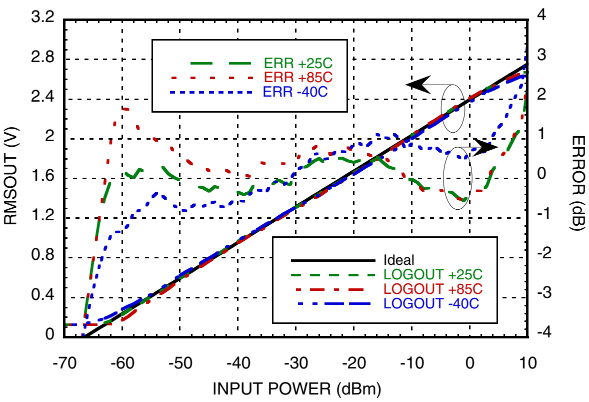
RMSOUT & Error vs. Pin @ 100 MHz [1][2]



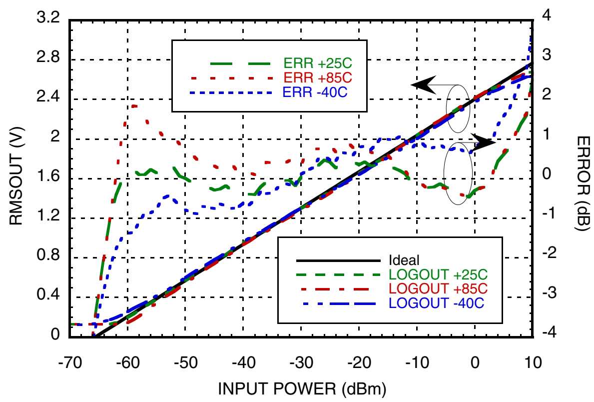
RMSOUT & Error vs. Pin @ 900 MHz [1][2]



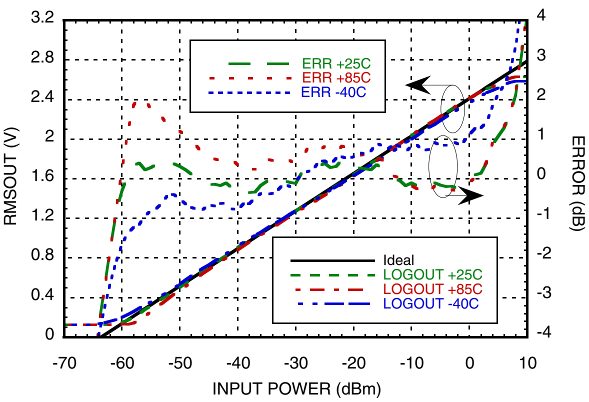
RMSOUT & Error vs. Pin @ 1900 MHz [1][2]



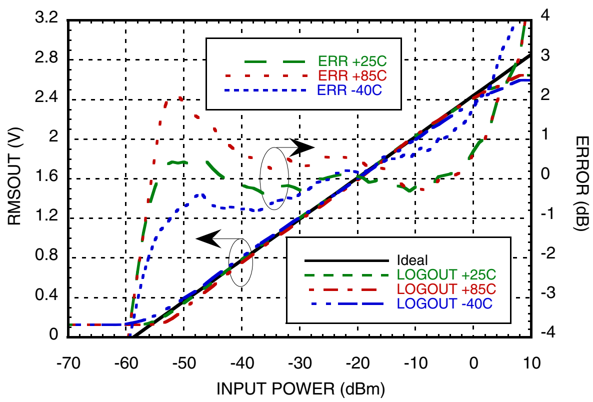
RMSOUT & Error vs. Pin @ 2200 MHz [1][2]



RMSOUT & Error vs. Pin @ 2700 MHz [1][2]



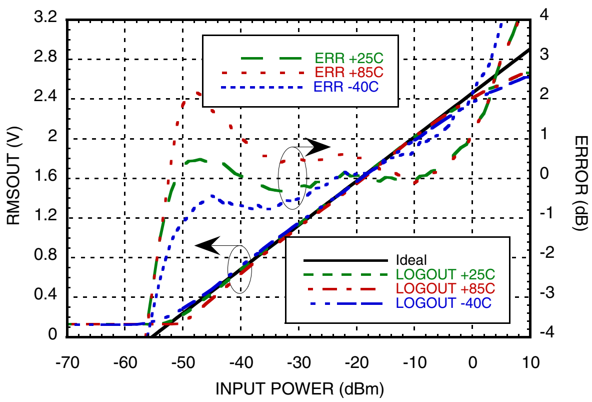
RMSOUT & Error vs. Pin @ 3500 MHz [1][2]



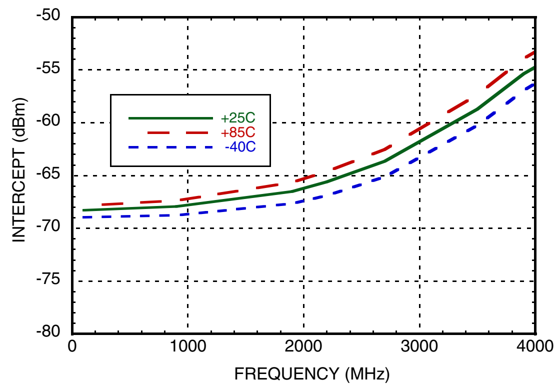
[1] Data was taken at Sci4=Sci1=0V, Sci3=Sci2=5V, shortest integration time is for SCI=0000, allowed longest integration time is for SCI=1100

[2] WCDMA 4 carriers input waveform

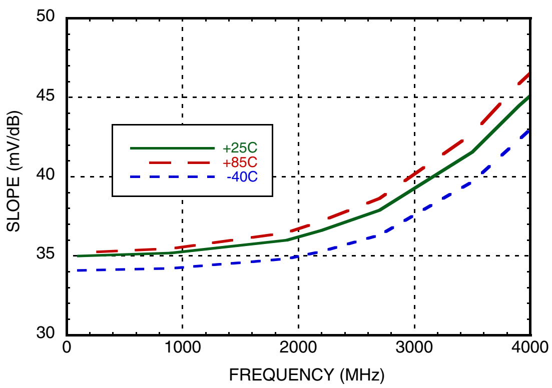
RMSOUT & Error vs. Pin @ 3900 MHz [1][2]



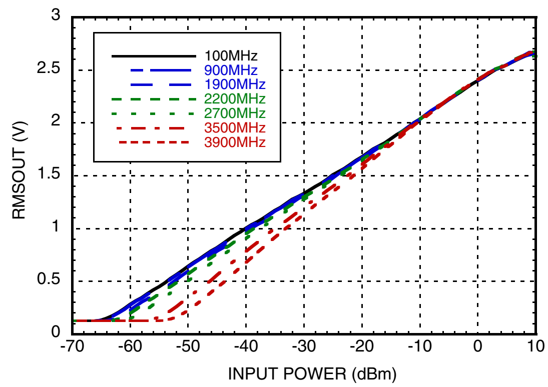
Intercept vs. Frequency [1][2]



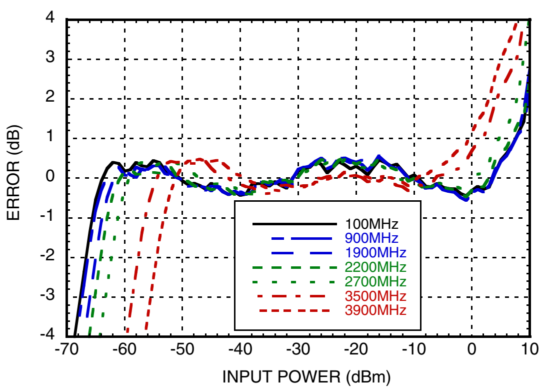
Slope vs. Frequency [1][2]



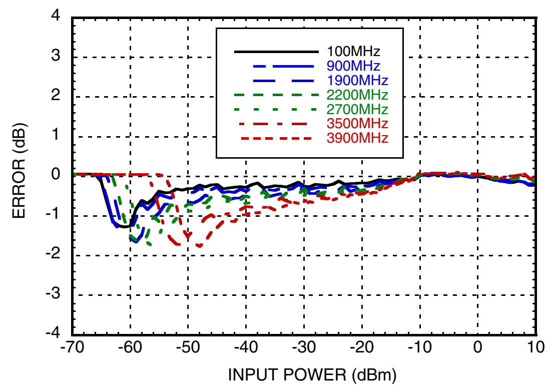
RMSOUT vs. Pin with WCDMA 4 Carrier @ +25 °C [1]



RMSOUT Error vs. Pin with WCDMA 4 Carrier @ +25 °C [1]



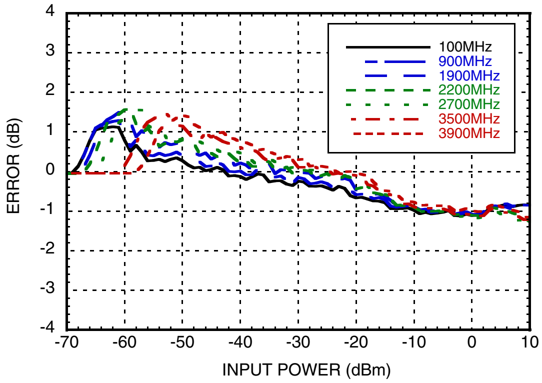
RMSOUT Error vs. Pin with WCDMA 4 Carrier @ +85 °C wrt +25 °C Response [1]



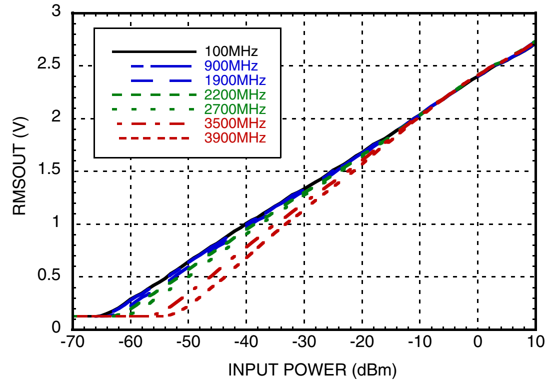
[1] Data was taken at Sci4=Sci1=0V, Sci3=Sci2=5V, shortest integration time is for SCI=0000, allowed longest integration time is for SCI=1100

[2] WCDMA 4 carriers input waveform

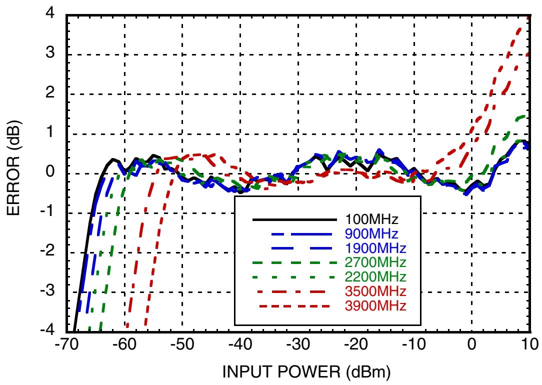
RMSOUT Error vs. Pin with WCDMA 4 Carrier @ -40 °C wrt +25 °C Response [1]



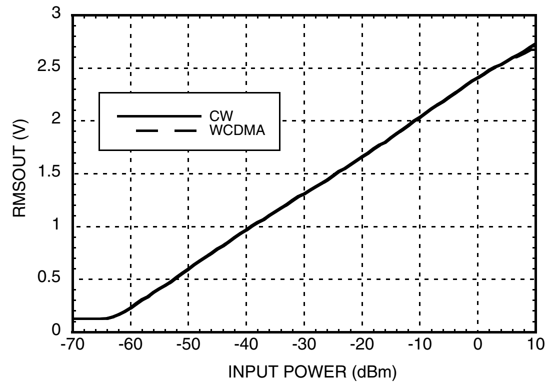
RMSOUT vs. Pin with CW @ +25 °C [1]



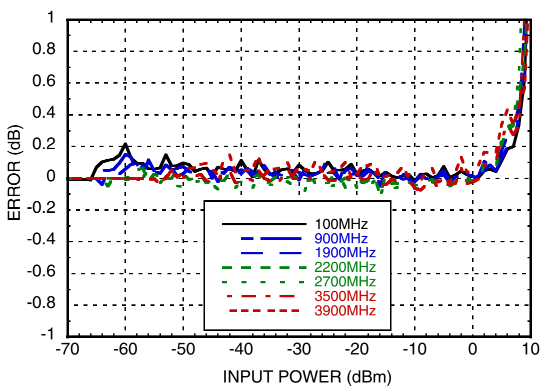
RMSOUT Error vs. Pin with CW @ +25 °C [1]



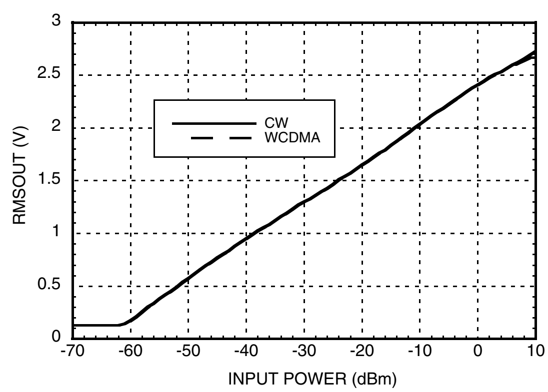
RMSOUT vs. Pin w/ CW & WCDMA 4 Carrier @ 1900 MHz & +25 °C [1]



Reading Error for WCDMA 4 Carrier wrt CW Response @ +25 °C [1]



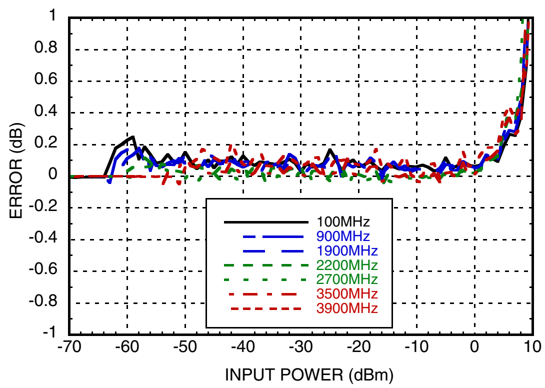
RMSOUT vs. Pin w/ CW & WCDMA 4 Carrier @ 1900 MHz & +85 °C [1]



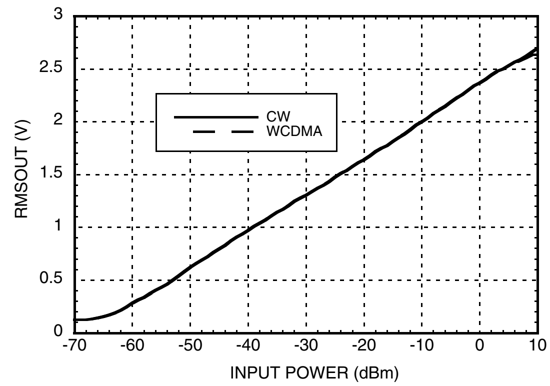
[1] Data was taken at Sci4=Sci1=0V, Sci3=Sci2=5V, shortest integration time is for SCI=0000, allowed longest integration time is for SCI=1100

RMS POWER DETECTOR SINGLE-ENDED, DC - 3.9 GHz

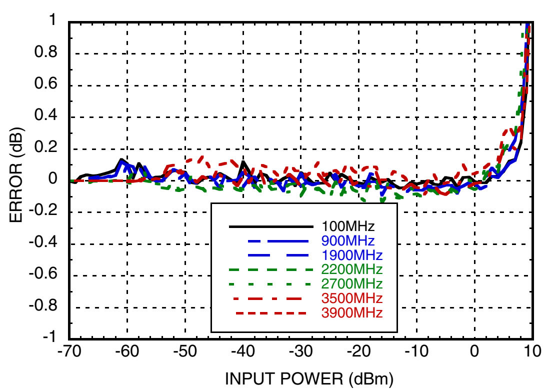
Reading Error for WCDMA 4 Carrier wrt CW Response @ +85 °C [1]



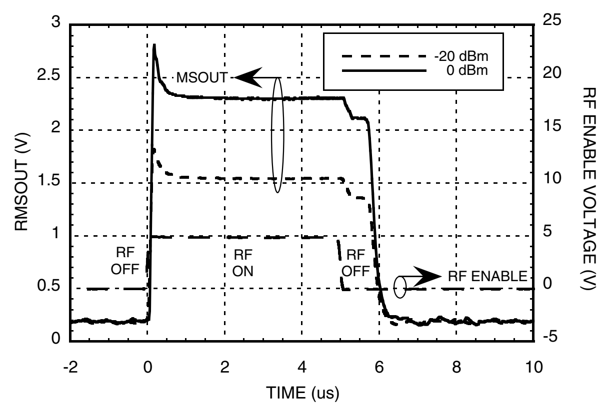
RMSOUT vs. Pin w/ CW & WCDMA 4 Carrier @ 1900 MHz & -40 °C [1]



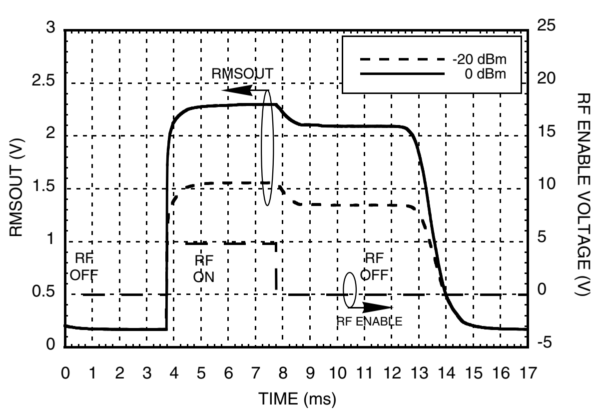
Reading Error for WCDMA 4 Carrier wrt CW Response @ -40 °C [1]



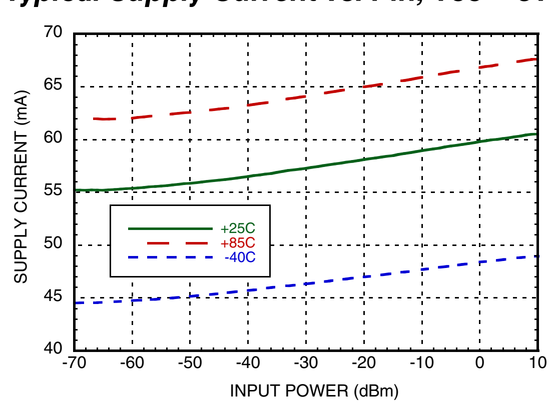
Output Response with SCI = 0000 @ 1900 MHz



Output Response with SCI = 1100 @ 1900 MHz



Typical Supply Current vs. Pin, Vcc = 5V



[1] Data was taken at Sci4=Sci1=0V, Sci3=Sci2=5V, shortest integration time is for SCI=0000, allowed longest integration time is for SCI=1100

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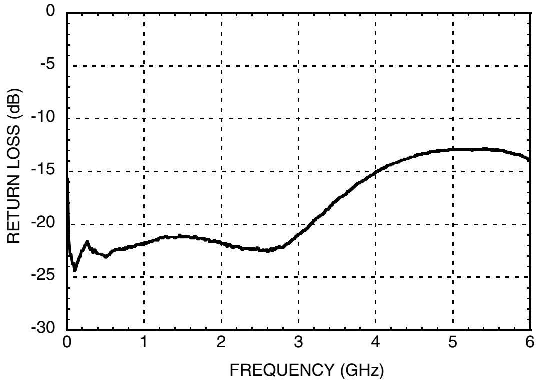
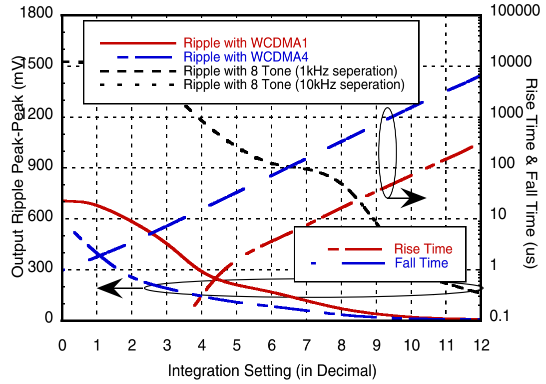
Phone: 978-250-3343 Fax: 978-250-3373 Order On-line at www.hittite.com
Application Support: Phone: 978-250-3343 or apps@hittite.com

Input Return Loss vs. Frequency



Output Ripple & Rise/Fall Time vs. Integration Setting [Sci4,Sci3,Sci2,Sci1] in Decimal



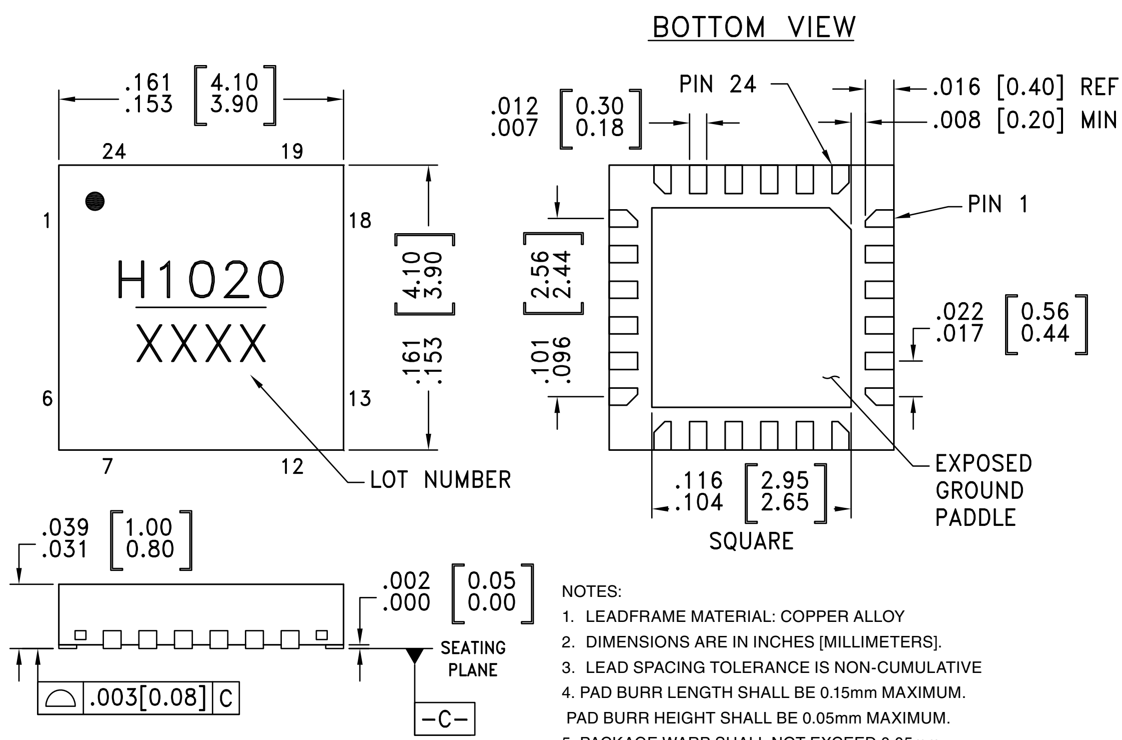
RoHS ✓ EARTH FRIENDLY

Absolute Maximum Ratings

Power Supply Voltage (Vcc)	5.6V
Single Ended RF Input Power	10 dBm
Single Ended Input Voltage	VCC ± 0.6V
Junction Temperature	125 °C
Continuous Pdiss (T = 85°C) (Derate 32.45 mW/°C above 85°C)	1.39 W
Thermal Resistance (R_{th}) (junction to ground paddle)	28.68 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1B

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HMC APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
HMC1020LP4E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H1020 XXXX

[1] 4-Digit lot number XXXX
[2] Max peak reflow temperature of 260 °C

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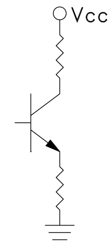
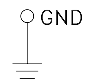
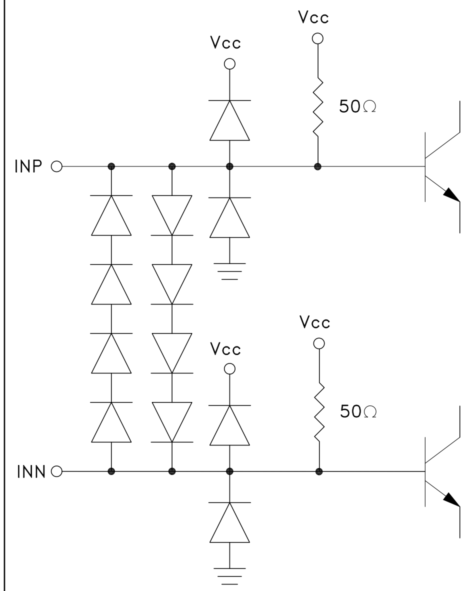
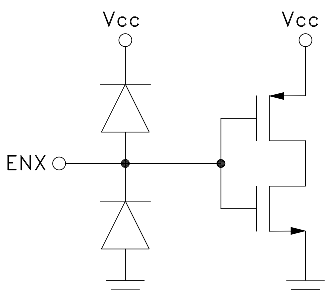
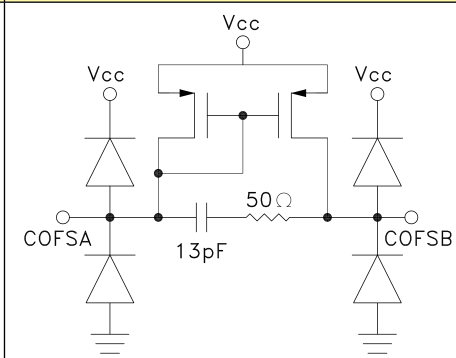
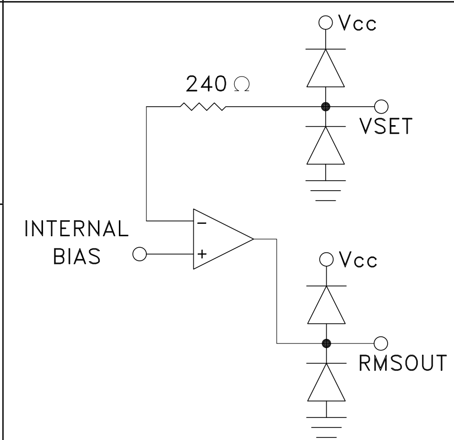
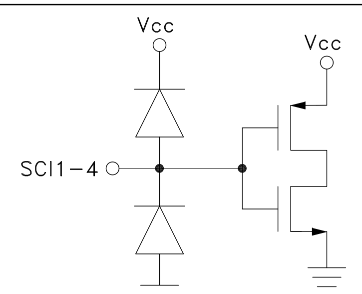
Phone: 978-250-3343 Fax: 978-250-3373 Order On-line at www.hittite.com
Application Support: Phone: 978-250-3343 or apps@hittite.com

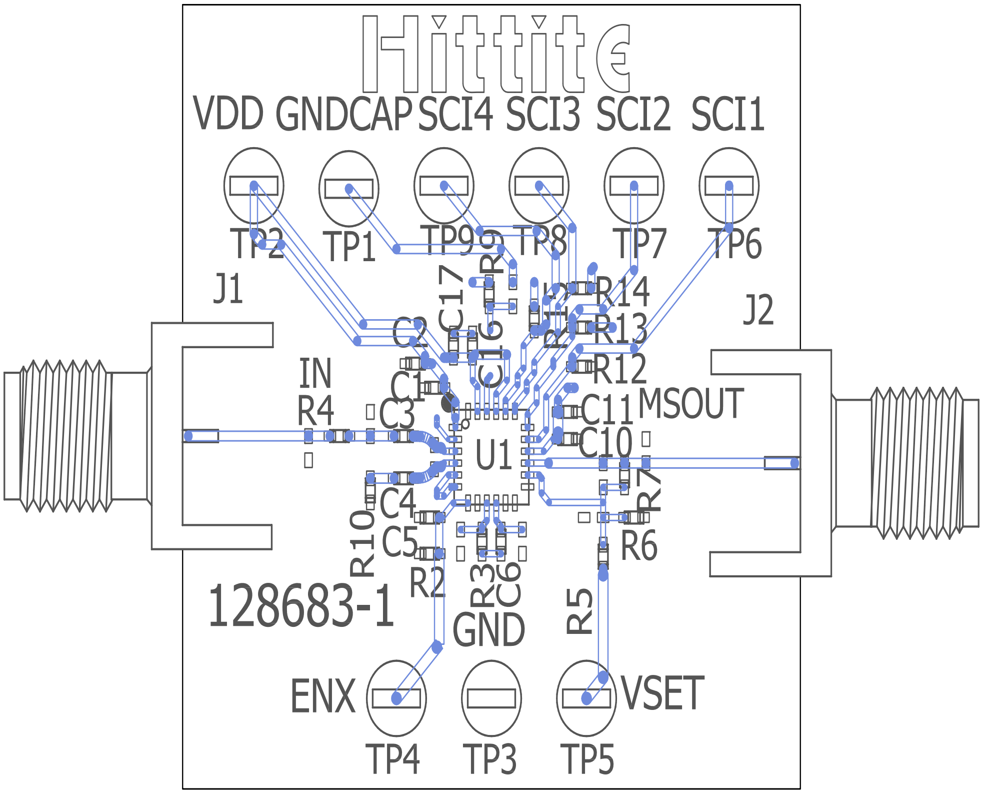
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 16, 21, 23	Vcc	Bias Supply. Connect supply voltage to these pins with appropriate filtering.	
2, 5, 6, 8, 11 - 13, 22, 24 Package Base	GND	Package bottom has an exposed metal paddle that must be connected to RF/DC ground.	
3 ,4	INP, INN	RF input pins.	
7	ENX	Disable pin. Connect to GND for normal operation. Applying voltage V>0.8xVcc will initiate power saving mode.	

Pin Descriptions (Continued)

Pin Number	Function	Description	Interface Schematic
9, 10	COFSA, COFSB	Input high pass filter capacitor. Connect a capacitor between COFSA and COFSB to determine 3 dB point of input signal high-pass filter.	
14	VSET	Set input point for controller mode.	
15	RMSOUT	Logarithmic output that provides an indication of mean square input power.	
17, 18, 19, 20	SCI1, SCI2, SCI3, SCI4	Digital input pins that control the internal integration time constant for mean square calculation. SCI4 is the most significant bit. Set V>0.2xVcc to disable. Shortest integration time is for SCI=0000, allowed longest integration time is for SCI=1100 (1101, 1110 and 1111 SCI settings are forbidden states). Each step changes the integration time by 1 octave.	

Evaluation PCB



List of Materials for Evaluation PCB

Item	Description
J1, J2	SMA Connector
TP1 - TP9	DC Pin
C1, C10, C16	100 pF Capacitor, 0402 Pkg.
C2, C5, C11, C17	100 nF Capacitor, 0402 Pkg.
C3, C4, C6	1000 pF Capacitor, 0402 Pkg.
R2, R12 - R15	10K Ohm Resistor, 0402 Pkg.
R3 - R5, R9, R10	0 Ohm Resistor, 0402 Pkg.
R6, R7	4.7K Ohm Resistor, 0402 Pkg.
U1	HMC1020LP4E RMS Power Detector
PCB [1]	128683-1 Evaluation PCB

[1] Circuit Board Material: Rogers 4350 or Arlon 25FR

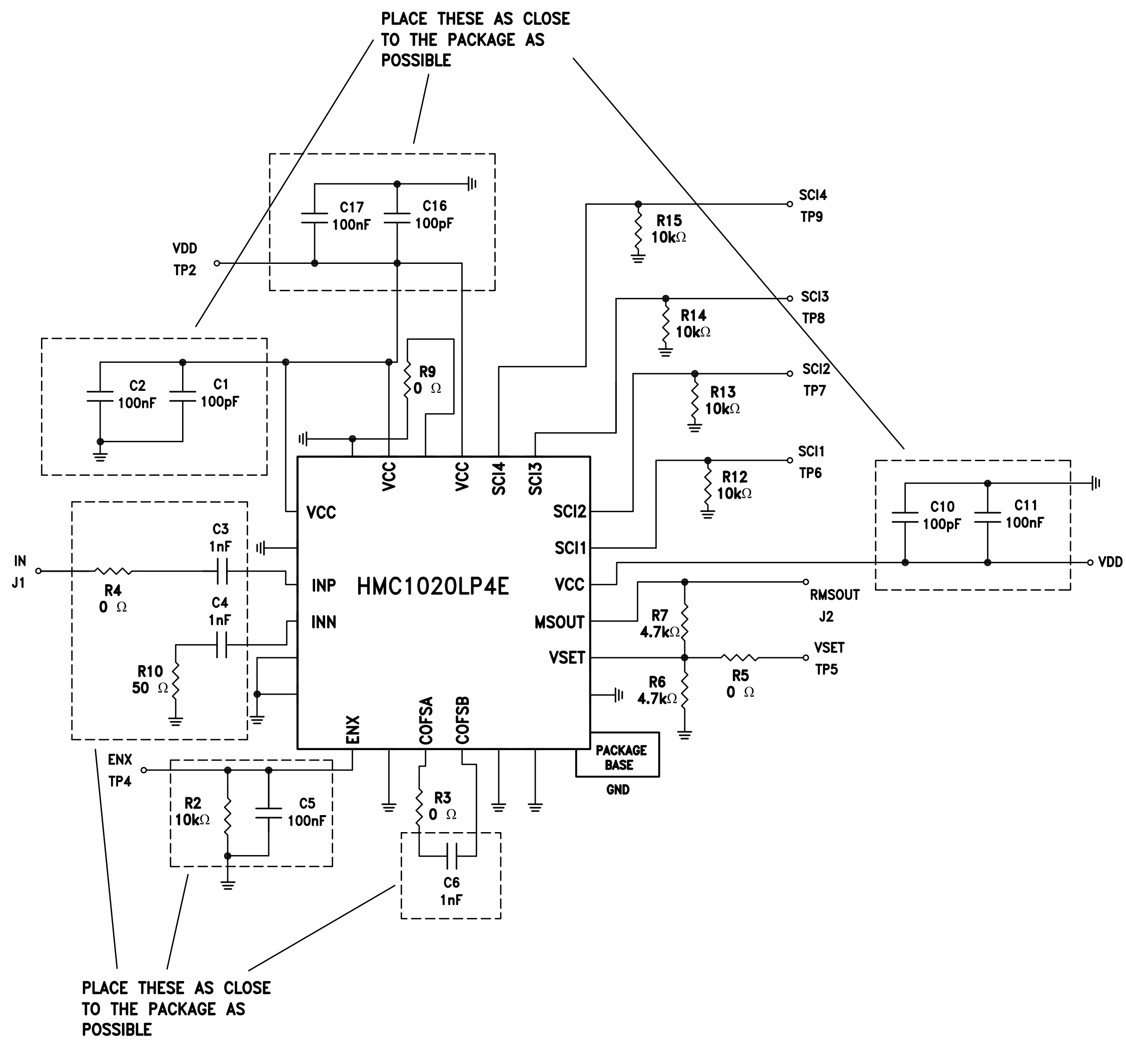
The circuit board used in the application should use RF circuit design techniques. Signal lines sho-uld have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Board is configured with wideband single-ended input interface suitable for input signal frequencies above 100 MHz. Refer to wideband single-ended input interface section in application information for operating with signals below 100 MHz.

Evaluation Order Information

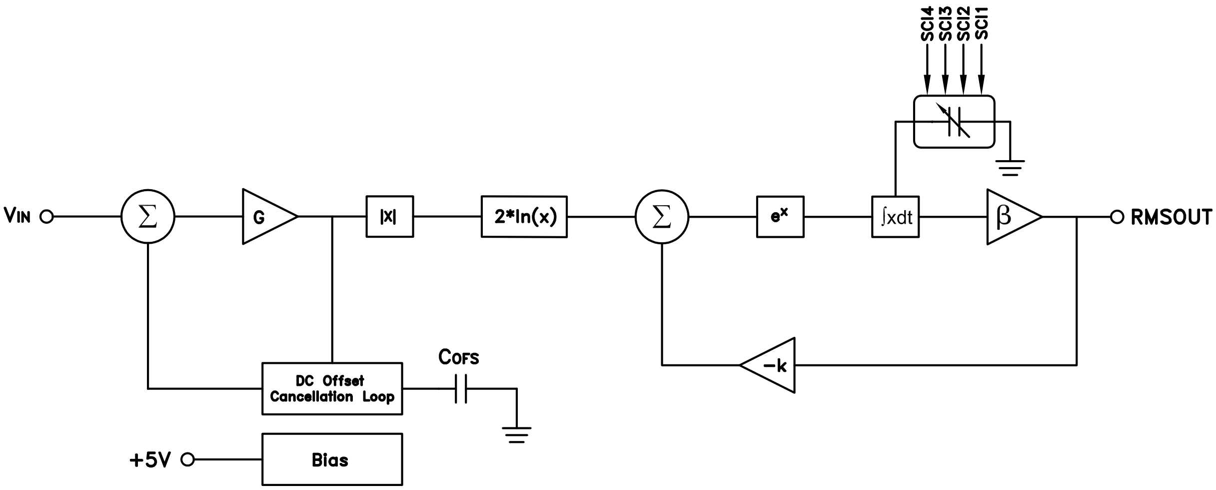
Item	Content	Part Number
Evaluation PCB	HMC1020LP4E Evaluation PCB	EVAL01-HMC1020LP4E

Application Circuit



Application Information

Principle of Operation



The HMC1020LP4E power detector is the optimal solution for monitoring and controlling transmitted and received signal power, measuring the incident RF signal power, and then generating an output signal representing the input power level.

The HMC1020LP4E is a monolithic true-RMS detector, which in fact is an analog calculator, designed to measure the actual RMS power of the input signal, independent of the modulated signal waveform complexity or modulation scheme. At the core of an RMS detector is a full-wave rectifier, log/antilog circuit, and an integrator. The RMS output signal is directly proportional to the logarithm of the time-average of V_{IN}^2. The bias block also contains temperature compensation circuits which stabilize output accuracy over the entire operating temperature range. The DC offset cancellation circuit actively cancels internal offsets so that even very small input signal levels can be measured accurately.

The HMC1020LP4E achieves exceptional RF power measurement accuracy independent of the modulation of the carrier, with the system architecture shown in the block diagram figure. The relation between the HMC1020LP4E's RMSOUT output and the RF input power is given below:

$$RMSOUT = \frac{1}{k}\ln\left(\beta k G^2 \int V_{IN}^{\,2} dt\right)$$

P_{IN} = RMSOUT / [log-slope] + [log-intercept], dBm

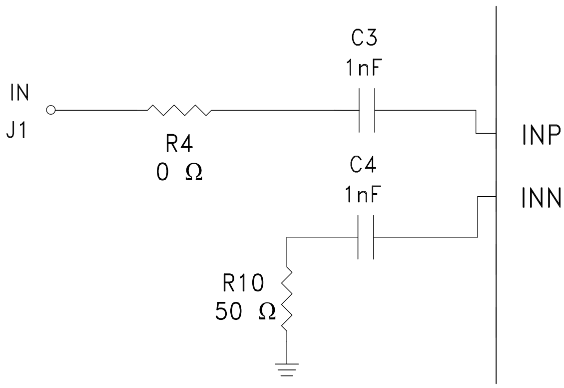
Configuration For The Typical Application

The HMC1020LP4E is a logarithmic RMS detector that can be directly driven with a single-ended 50-Ohm RF source. The integrated broadband single-ended input interface of HMC1020LP4E eliminates the requirement for an external balun transformer or a matching network. The HMC1020LP4E can be operated from DC to 3.9 GHz by using only standard DC blocking capacitors. This simple input interface provides cost and PCB area reductions and increases measurement repeatability.

The RMS output signal is typically connected to VSET through a resistive network providing a Pin -> RMSOUT transfer characteristic slope of 35.2 mV/dB (at 900 MHz). However the RMS output can be re-scaled to "magnify" a specific portion of the input sensing range, and to fully utilize the dynamic range of the RMS output. Refer to the section under the "log-slope and intercept" heading for details.

Due to part-to-part variations in log-slope and log-intercept, a system-level calibration is recommended to satisfy absolute accuracy requirements; refer to the "System Calibration" section for more details.

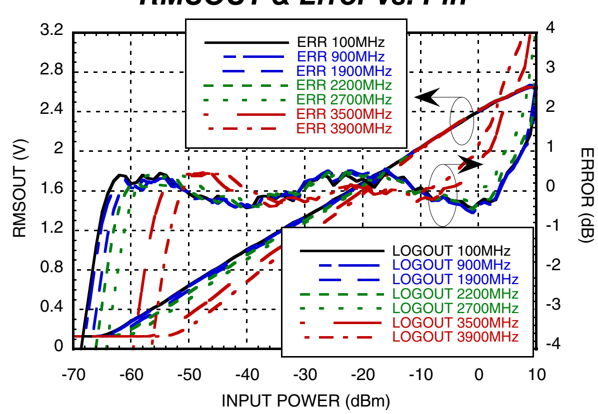
Broadband Single-Ended Input Interface



The HMC1020LP4E operates with a single-ended input interface and requires only two external DC blocking capacitors and an external 50 Ohm resistor. The HMC1020LP4E input interface shown below provides a compact, broadband solution.

Note that the provided single-ended input interface covers the whole operating spectrum of the HMC1020LP4E and does not require matching/tuning for different frequencies. The performance of the HMC1020LP4E at different frequencies is shown below:

RMSOUT & Error vs. Pin



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RMS Output Interface and Transient Response

The HMC1020LP4E features digital input pins (SCI1-SCI4) that control the internal integration time constant. Output transient response is determined by the digital integration controls, and output load conditions.

Shortest integration time is for SCI=0000, allowed longest integration time is for SCI=1100 (1101, 1110 and 1111 SCI settings are forbidden states).

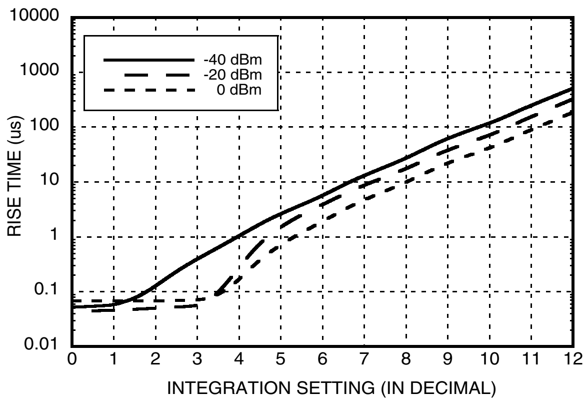
Using larger values of SCI will narrow the operating bandwidth of the integrator, resulting in a longer averaging time interval and a more filtered output signal. It will also slow the power detector's transient response. A larger SCI value favors output accuracy over speed. For the fastest possible transient settling times set SCI to 0000. This configuration will operate the integrator at its widest possible bandwidth, resulting in short averaging time-interval and an output signal with little filtering. For most applications an SCI setting may be selected to maintain a balance between speed and accuracy. Furthermore, error performance over modulation bandwidth is dependent on the SCI setting. For example, modulations with relatively low frequency components and high crest factors may require higher SCI (integration) settings.

Table 1: Transient Response vs. SCI Setting [1]:

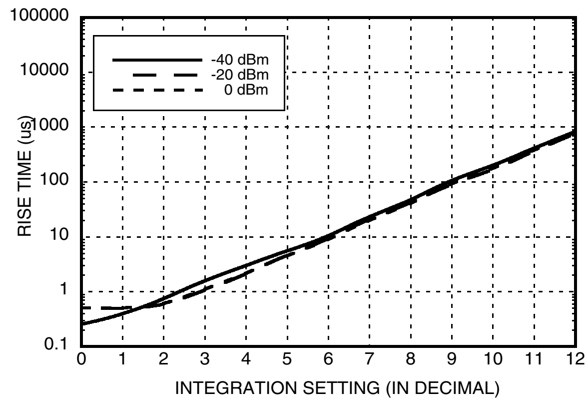
	RMSOUT Rise-Time 10% -> 90% (µs) [3]			RMSOUT Rise Settling Time (µs) [2]			RMSOUT Fall-time 100% -> 10% (µs) [4]		
SCI4,3,2,1	Pin = 0 dBm	Pin = -20 dBm	Pin = -40 dBm	Pin = 0 dBm	Pin = -20 dBm	Pin = -40 dBm	Pin = 0 dBm	Pin = -20 dBm	Pin = -40 dBm
0000	0.0686	0.044	0.053	0.509	0.504	0.257	0.969	0.975	1
0010	0.0684	0.05	0.093	0.54	0.524	0.6788	2.98	3.193	3.35
0100	0.076	0.066	0.878	1.956	1.872	2.82	13.5	14.18	14.978
0110	1.624	3.432	4.84	7.8	8.056	8.92	62.9	65.384	69.224
1000	8.6	15.32	23.4	35.52	37.28	40.92	294.64	304.52	317.32
1010	38.6	65.8	109.6	165.2	156	188	1379.4	1423.6	1477.6
1100	186	325	509	802	770	831	6447	6640	6881

[1] Input signal is 1900 MHz CW -tone switched on and off
[2] Measured from RF switching edge to 1dB (input referred) settling of RMSOUT.
[3] Measured from 10% to 90%
[4] Measured from 100% to 10%

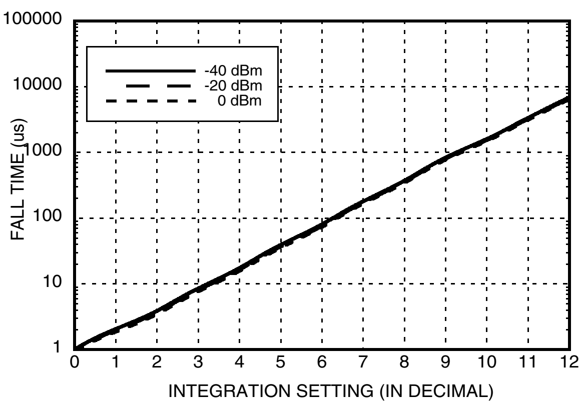
Rise Time[1] vs. SCI Setting over Input Power



Rise Settling Time[2] vs. SCI Setting over Input Power



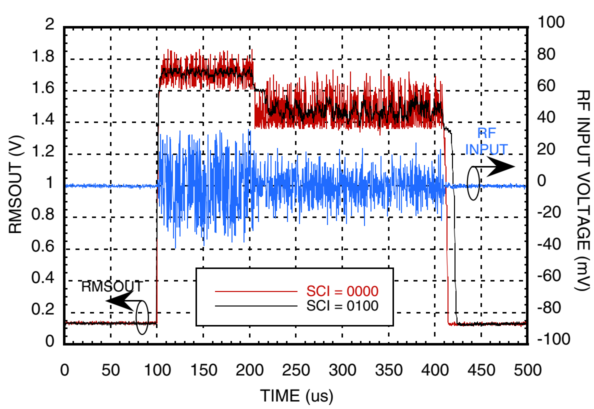
Fall Time[1] vs. SCI Setting over Input Power



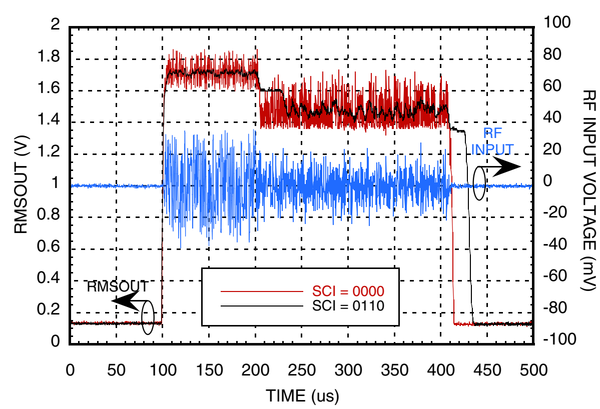
For increased load drive capability, consider a buffer amplifier on the RMS output. Using an integrating amplifier on the RMS output allows for an alternative treatment for faster settling times. An external amplifier optimized for transient settling can also provide additional RMS filtering, when operating HMC1020LP4E with a lower SCI value.

Following figures show how the peak-to-peak ripple decreases with higher SCI settings along with the RF pulse response over different modulations.

Residual Ripple for 900 Mhz WiMAX @ SCI=0100



Residual Ripple for 900 Mhz WiMAX @ SCI=0110

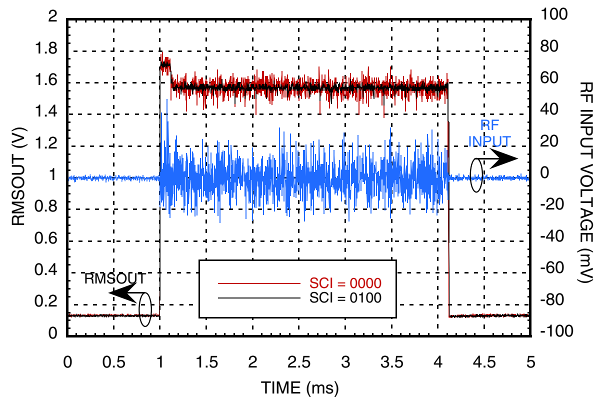


[1] Measured from 10% to 90%

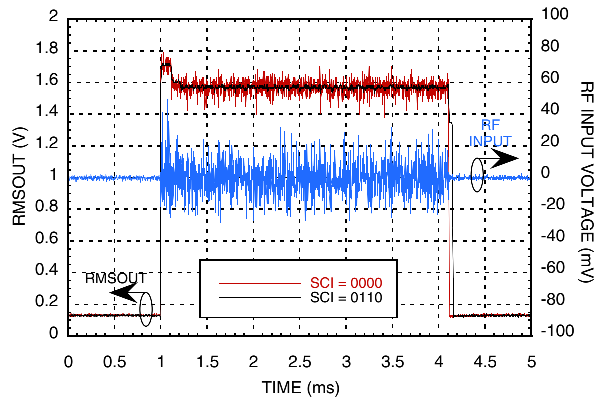
[2] Measured from RF switching edge to 1dB (input referred) settling of RMSOUT.

[3] Measured from 100% to 10%

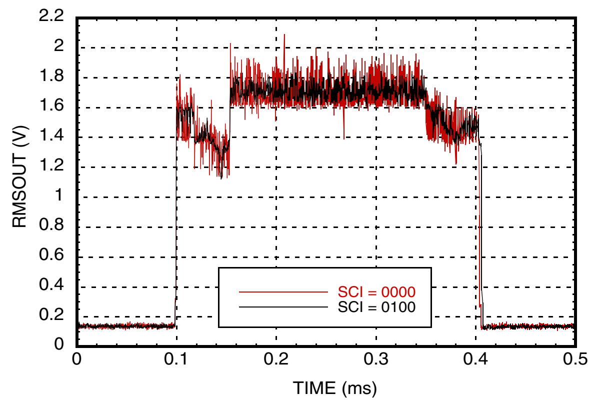
Residual Ripple for 900 Mhz WiBRO @ SCI=0100



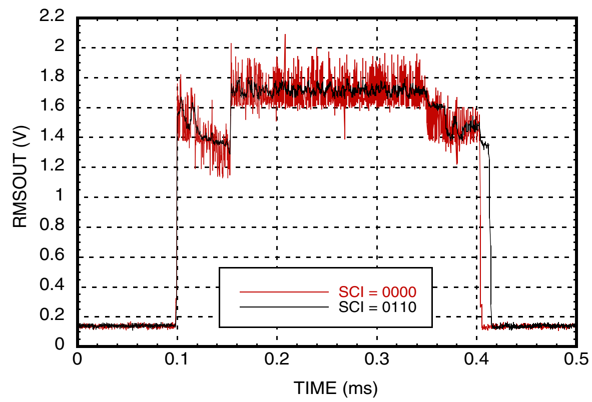
Residual Ripple for 900 Mhz WiBRO @ SCI=0110



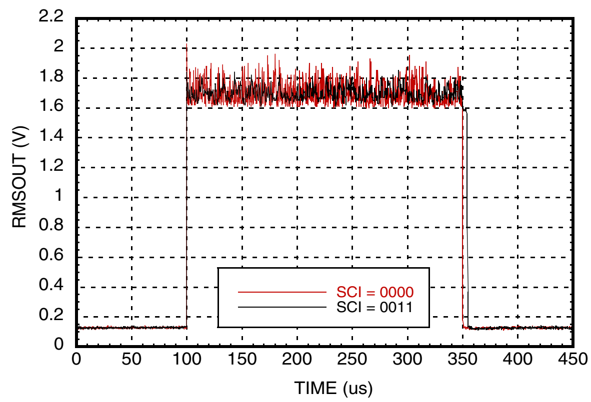
Residual Ripple for 900 Mhz LTE Downlink @ SCI=0100



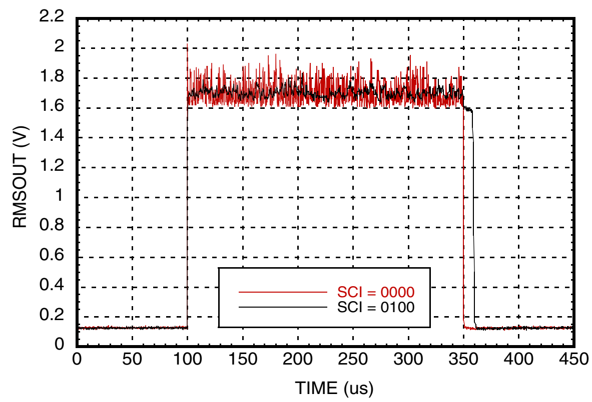
Residual Ripple for 900 Mhz LTE Downlink @ SCI=0110



Residual Ripple for 900 Mhz WCDMA4 @ SCI=0011



Residual Ripple for 900 Mhz WCDMA4 @ SCI=0100

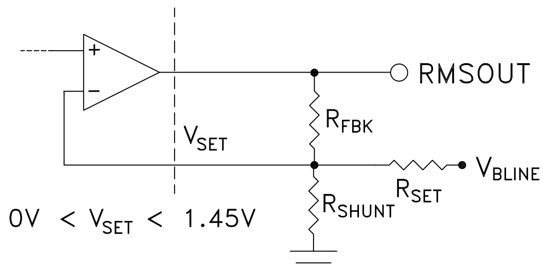


LOG-Slope and Intercept

The HMC1020LP4E provides for an adjustment of output scale with the use of an integrated operational amplifier. Logarithmic slope and intercept can be adjusted to “magnify” a specific portion of the input sensing range, and to fully utilize the dynamic range of the RMS output.

A log-slope of 35.2 mV/dB (@1900 MHz) is set by connecting RMS Output to VSET through a resistor network for ß=1 (see application schematic).

The log-slope is adjusted by applying the appropriate resistors on the RMS and VSET pins. Log-intercept is adjusted by applying a DC voltage to the VSET pin.



Optimized slope = ß * log-slope

Optimized intercept = log_intercept – (R_{FBK} /R_{SET}) * V_{BLINE}

$$\beta = \frac{1}{2}\,\frac{R_{FBK}}{R_{FBK} \,//\, R_{SHUNT} \,//\, R_{SET}}$$

When R_{FBK}=0 to set RMSOUT=V_{SET}, then ß=1/2

If R_{SET} is not populated, then ß = ½ * (R_{FBK}/ (R_{FBK} // R_{SHUNT})) and intercept is at nominal value.

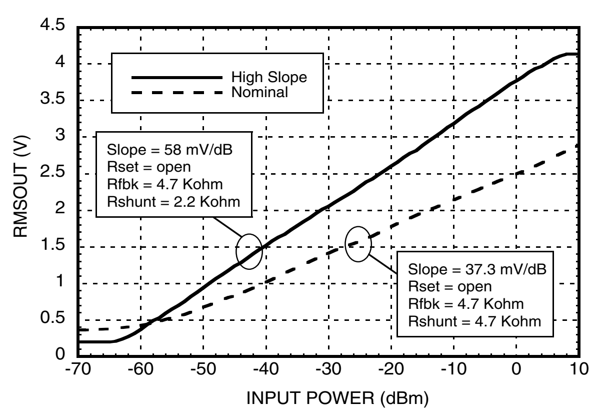
Example: The logarithmic slope can be simply increased by choosing appropriate R_{FBK} and R_{SHUNT} values while not populating the RSET resistor on the evaluation board to keep the intercept at nominal value.

Setting R_{FBK} =4.7KΩ and R_{SHUNT} = 2.2KΩ results in an optimized slope of:

Optimized Slope = ß * log_slope = 1.57* 36.9mV / dB

Optimized Slope = 58 mV / dB

Slope Adjustment



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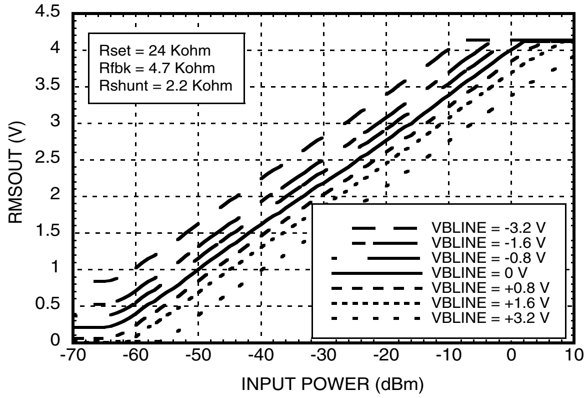
Intercept Adjustment



DC Offset Compensation Loop

Internal DC offsets, which are input signal dependant, require continuous cancellation. Offset cancellation is a critical function needed for maintenance of measurement accuracy and sensitivity. The DC offset cancellation loop performs this function, and its response is largely defined by the capacitance (COFS) connected between COFSA, COFS pins.

C_{OFS} capacitor sets the loop bandwidth of the DC offset compensations. Higher C_{OFS} values are required for measuring lower RF frequencies. The optimal loop bandwidth setting will allow internal offsets to be cancelled at a minimally acceptable speed.

DC Offset Cancellation Loop $\approx \dfrac{1}{\pi(5000)(C_{OFS}+20\times10^{12})}$ Bandwidth , Hz

For example: loop bandwidth for DC cancellation with C_{OFS} = 1nF, bandwidth is ~62 kHz

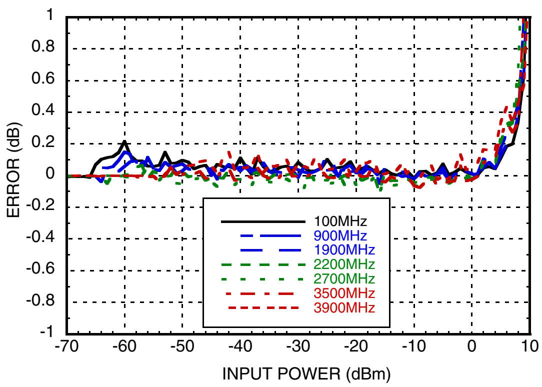
Standby Mode

The ENX pin can be used to force the power detector into a low-power standby mode. As ENX is deactivated, power is restored to all of the circuits. There is no memory of previous conditions. Coming out of standby mode, internal integration and COFS capacitors will require recharging, so if large SCI values have been chosen, the wake-up time will be lengthened.

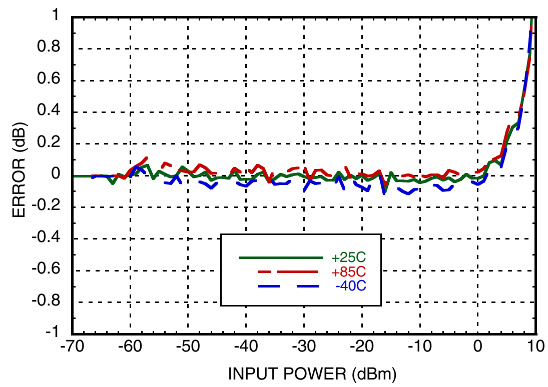
Modulation Performance – Crest factor performance

The HMC1020LP4E is capable of detecting the average power of RF signals with complex modulation schemes with exceptional accuracy. The proprietary RMS detection core is optimized to accurately detect the RMS power of the modulated RF signals with very high crest factors. This crest factor immune detection architecture of HMC1020LP4E results in detection accuracy of better than 0.2 dB over the entire operating frequency and temperature range. The response of the HMC1020LP4E to a WCDMA4TM test signal is compared with the CW response in the following plots:

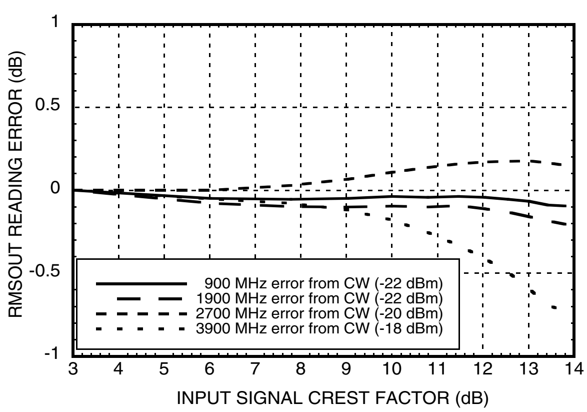
Reading Error for WCDMA 4 Carrier wrt CW Response @ +25 °C



Reading Error for WCDMA 4 Carrier wrt CW Response @ 2200MHz



RMSOUT Error vs. Crest Factor over Frequency



System Calibration

Due to part-to-part variations in log-slope and log-intercept, a system-level calibration is recommended to satisfy absolute accuracy requirements. When performing this calibration, two test points near the top end and bottom-end of the desired detection dynamic range should be chosen. It is best to measure the calibration points in the regions (of frequency and amplitude) where accuracy is most important. The log-slope and log-intercept parameters should be derived and then stored in nonvolatile memory. These parameters relate the RMSOUT output voltage reading of HMC1020LP4E to the actual RMS power level as shown below:

P_{IN} = RMSOUT / [log-slope] + [log-intercept], dBm

The derivation procedure of the log-slope and log-intercept parameters is elaborated below:

For example if the following two calibration points were measured at 2.2 GHz:

With RMSOUT = 2.0338V at Pin = -10 dBm,
and RMSOUT = 0.5967V at Pin = -50 dBm
slope calibration constant = SCC
SCC = = (-50+10)/(0.5967-2.0338) =27.83 dB/V
intercept calibration constant = ICC
ICC = Pin – SCC *RMSOUT = -10 – 27.83 * 2.0338 = -66.60 dBm

Now performing a power measurement at -30 dBm:

RMSOUT measures 1.3089V
[Measured Pin] = [Measured RMSOUT]*SCC + ICC
[Measured Pin] = 1.3089*27.83 – 66.60 = -30.17 dBm
An error of only 0.17 dB

Factory system calibration measurements should be made using an input signal representative of the application. If the power detector is intended to operate over a wide range of frequencies, then a central frequency should be chosen for calibration.

Layout Considerations

- Mount RF input coupling capacitors close to the INP and INP pins.
- Solder the heat slug on the package underside to a grounded island which can draw heat away from the die with low thermal impedance. The grounded island should be at RF ground potential.
- Connect power detector ground to the RF ground plane, and mount the supply decoupling capacitors close to the supply pins.

Definitions

- Log-slope: slope of P_{IN} –> RMSOUT transfer characteristic. In units of mV/dB
- Log-intercept: x-axis intercept of P_{IN} –> RMSOUT transfer characteristic. In units of dBm.
- RMS Output Error: The difference between the measured P_{IN} and actual P_{IN} using a line of best fit.

[measured_P_{IN}] = [measured_ RMSOUT] / [best-fit-slope] + [best-fit-intercept], dBm

- Input Dynamic Range: the range of average input power for which there is a corresponding RMS output voltage with "RMS Output Error" falling within a specific error tolerance.
- Crest Factor: Peak power to average power ratio for time-varying signals.