Document Number: AFT18HW355S
Rev. 1, 1/2013

RoHS

RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 63 watt asymmetrical Doherty RF power LDMOS transistor is designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 1805 to 1880 MHz.

- Typical Doherty Single-Carrier W-CDMA Performance: V_{DD} = 28 Volts, I_{DQA} = 1100 mA, V_{GSB} = 1.45 Vdc, P_{out} = 63 Watts Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

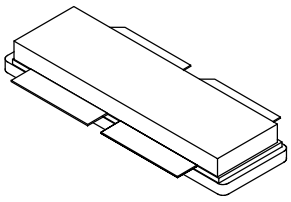
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
1805 MHz	14.8	48.1	7.3	-27.2	-13
1840 MHz	15.3	48.9	7.4	-27.7	-12
1880 MHz	15.2	48.3	7.5	-29.2	-9

Features

- Advanced High Performance In-Package Doherty
- Designed for Wide Instantaneous Bandwidth Applications
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- In Tape and Reel. R6 Suffix = 150 Units, 56 mm Tape Width, 13-inch Reel. For R5 Tape and Reel option, see p. 15.

AFT18HW355SR6

1805-1880 MHz, 63 W AVG., 28 V



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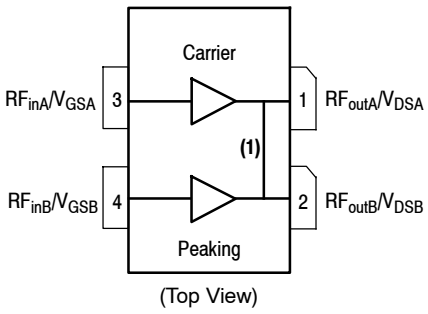

Figure 1. Pin Connections

1. Pin connections 1 and 2 are DC coupled and RF independent.

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freescale Airfast

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature Range	T_C	-40 to +125	°C
Operating Junction Temperature Range (1,2)	T_J	-40 to +225	°C
CW Operation @ T_C = 25°C Derate above 25°C	CW	259 0.64	W W/°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 77°C, 63 W CW, 28 Vdc, I_{DQA} = 1100 mA, V_{GSB} = 1.45 Vdc, 1840 MHz Case Temperature 106°C, 225 W CW(4), 28 Vdc, I_{DQA} = 1100 mA, V_{GSB} = 1.45 Vdc, 1840 MHz	$R_{\theta JC}$	 0.47 0.30	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	B
Charge Device Model (per JESD22-C101)	IV

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (5)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	5	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics - Side A (5) (Carrier)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 146 μAdc)	$V_{GS(th)}$	1.6	2.1	2.6	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DA} = 1100 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	2.4	2.9	3.4	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1.5 Adc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc
On Characteristics - Side B (5) (Peaking)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 291 μAdc)	$V_{GS(th)}$	1.6	2.1	2.6	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 2.9 Adc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc

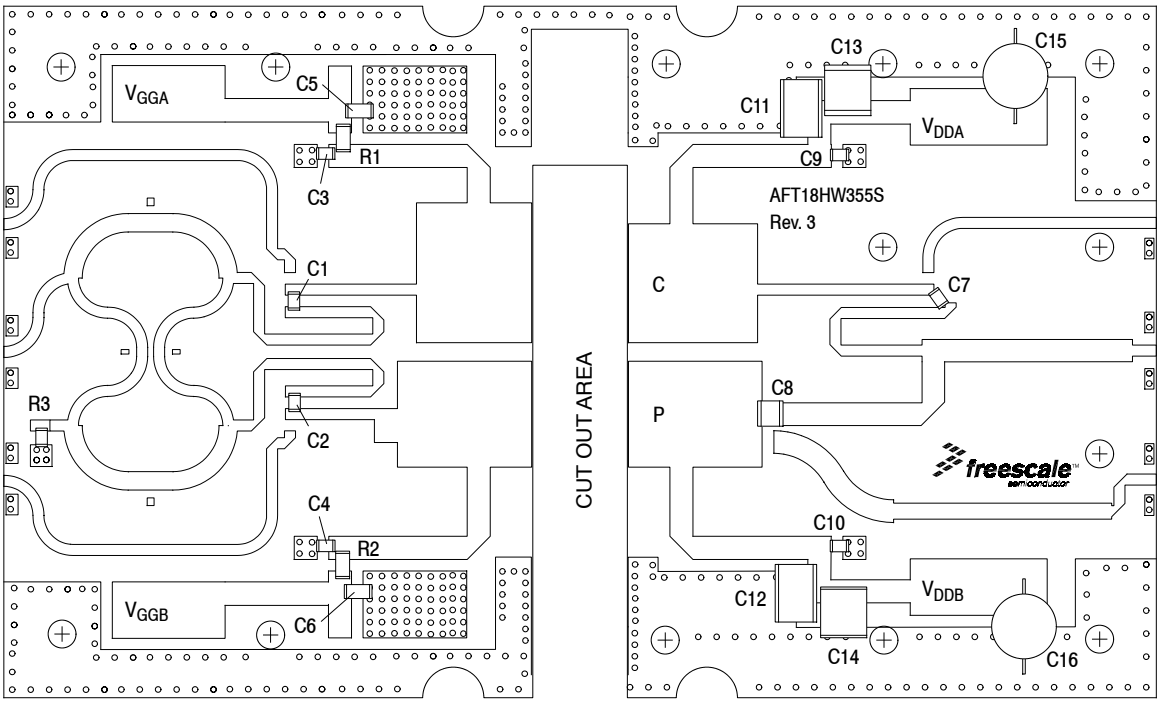
1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.
4. Exceeds recommended operating conditions. See CW operation data in Maximum Ratings table.
5. Each side of device measured separately.

(continued)

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1,2,3) (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 1100 mA, V_{GSB} = 1.45 Vdc, P_{out} = 63 W Avg., f = 1880 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	14.2	15.2	17.0	dB
Drain Efficiency	η_D	45.0	48.3	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	7.1	7.5	—	dB
Adjacent Channel Power Ratio	ACPR	—	-29.2	-26.0	dBc
Input Return Loss	IRL	—	-9	-8	dB
Load Mismatch (In Freescale Doherty Test Fixture, 50 ohm system) I_{DQA} = 1100 mA, V_{GSB} = 1.45 Vdc, f1 = 1795 MHz, f2 = 1895 MHz, 2-Carrier W-CDMA, 3.84 MHz Channel Bandwidth Carriers. PAR = 9.9 dB @ 0.01% Probability on CCDF.					
VSWR 10:1 at 32 Vdc, 252 W W-CDMA Output Power	No Device Degradation				
Typical Performances (2) (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 1100 mA, V_{GSB} = 1.45 Vdc, 1805-1880 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	350 (4,5)	—	W
P_{out} @ 3 dB Compression Point (6)	P3dB	—	400	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 1805-1880 MHz frequency range)	Φ	—	22	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	150	—	MHz
Gain Flatness in 75 MHz Bandwidth @ P_{out} = 63 W Avg.	G_F	—	0.63	—	dB
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.01	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C) (5)	ΔP1dB	—	0.013	—	dB/°C

1. Part internally matched both on input and output.
2. V_{DDA} and V_{DDB} must be tied together and powered by a single DC power supply.
3. Measurement made with device in an asymmetrical Doherty configuration.
4. Calculated from load pull P3dB measurements.
5. Exceeds recommended operating conditions. See CW operation data in Maximum Ratings table.
6. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.



Note 1: V_{DDA} and V_{DDB} must be tied together and powered by a single DC power supply.

Figure 2. AFT18HW355SR6 Test Circuit Component Layout

Table 5. AFT18HW355SR6 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C7, C9, C10	18 pF Chip Capacitors	GQM2195C2A180JB12D	Murata
C5, C6	2.2 μF Chip Capacitors	C1206C225K4RAC	Kemet
C8	8.2 pF Chip Capacitor	ATC100B8R2CT500XT	ATC
C11, C12	2.2 μF Chip Capacitors	C1825C225K5RAC	Kemet
C13, C14	22 μF Chip Capacitors	C5750Y5V1H226Z	TDK
C15, C16	470 μF, 63 V Electrolytic Capacitors	MCGPR63V477M13X26-RH	Multicomp
R1, R2	2.2 Ω, 1/4 W Chip Resistors	CRCW12062R20JNEA	Vishay
R3	50 Ω, 10 W Chip Resistor	81A7031-50-5F	Florida RF Labs
PCB	0.020″, ε_r = 3.5	RO4350B	Rogers

TYPICAL CHARACTERISTICS

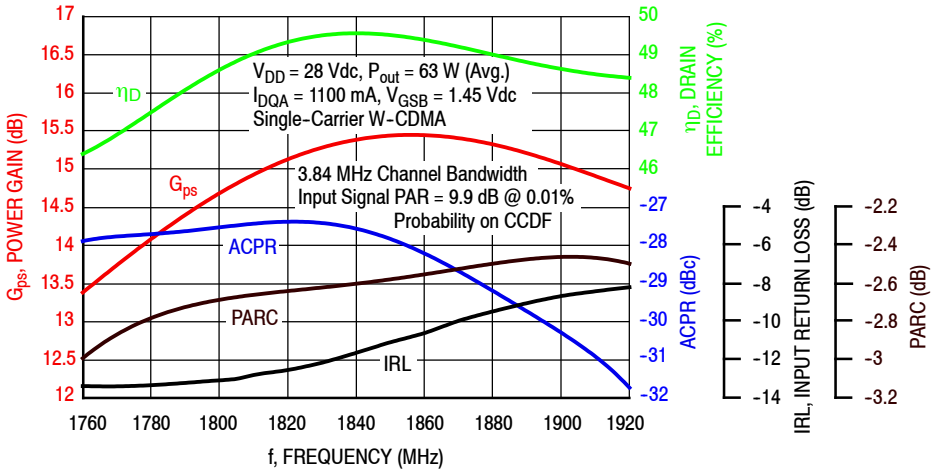


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 63 Watts Avg.

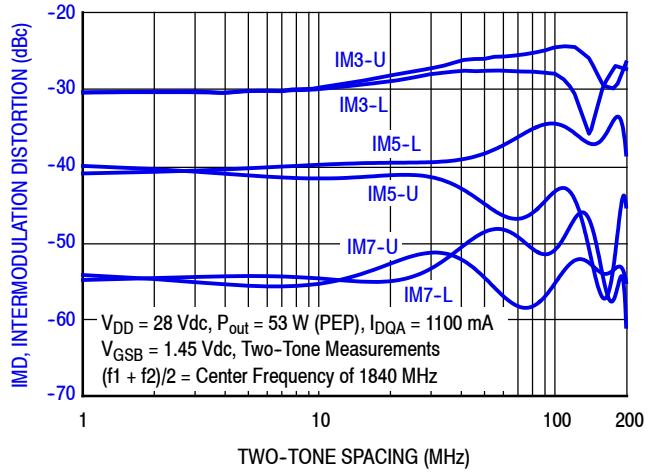


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

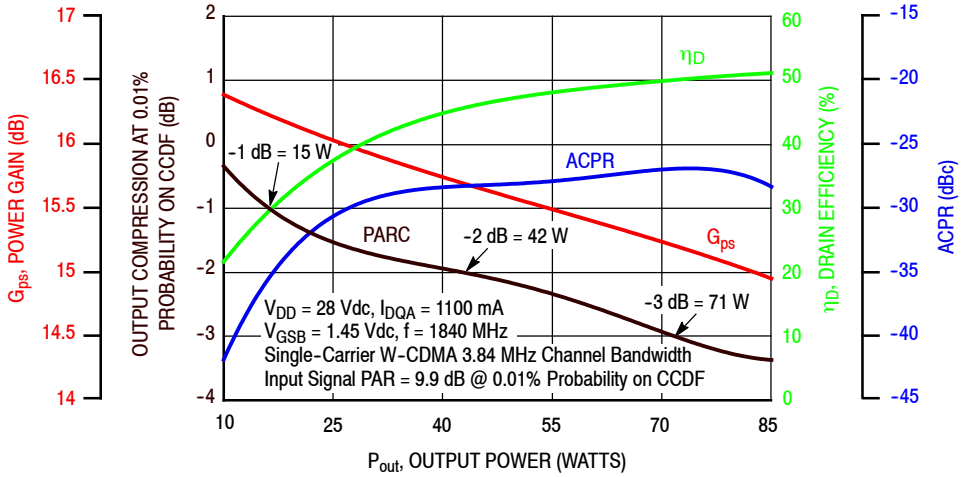


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

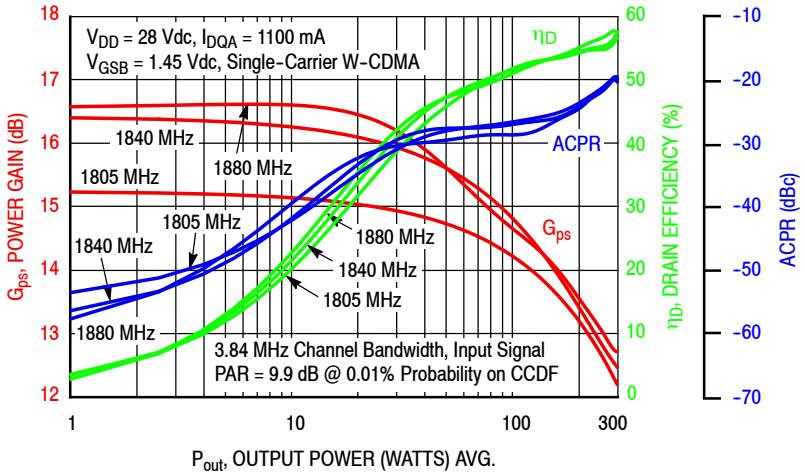


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

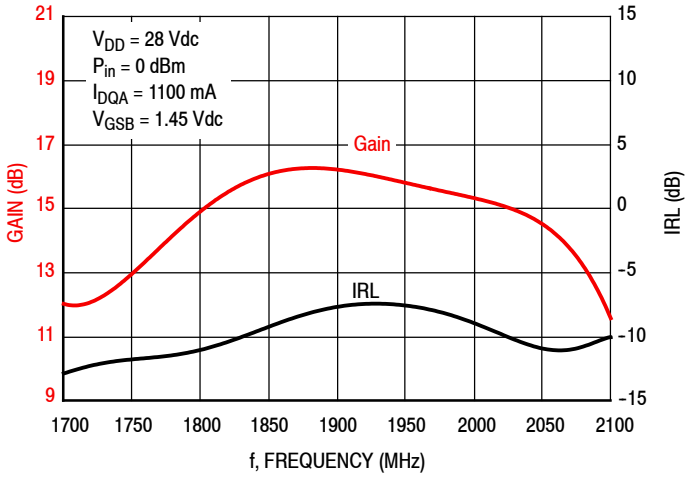


Figure 7. Broadband Frequency Response

V_{DD} = 28 Vdc, I_{DQA} = 1100 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Max Linear Gain (dB)	Max Output Power							
					P1dB				P3dB			
					(dBm)	(W)	η_D (%)	AM/PM (°)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	1.14 - j4.15	1.12 + j4.37	1.21 - j4.03	18.3	51.8	151	58.1	9.2	52.7	186	60.0	15
1840	1.14 - j4.41	1.32 + j4.55	1.24 - j4.24	18.4	51.6	145	57.4	9.1	52.6	182	59.4	16
1880	1.54 - j4.56	1.61 + j4.79	1.23 - j4.39	18.2	51.7	148	56.6	9.2	52.6	182	58.3	15

(1) Load impedance for optimum P1dB power.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

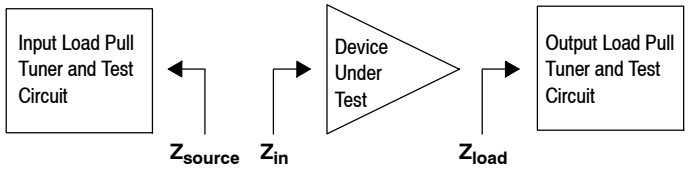


Figure 8. Carrier Side Load Pull Performance — Maximum P1dB Tuning

V_{DD} = 28 Vdc, I_{DQA} = 1100 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Max Linear Gain (dB)	Max Drain Efficiency							
					P1dB				P3dB			
					(dBm)	(W)	η_D (%)	AM/PM (°)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	1.14 - j4.15	1.08 + j4.44	2.56 - j3.08	21.1	49.9	98	69.8	15	50.6	115	71.8	24
1840	1.14 - j4.41	1.25 + j4.64	2.54 - j2.75	21.6	49.3	85	68.9	16	50.6	115	71.2	26
1880	1.54 - j4.56	1.53 + j4.87	2.30 - j3.10	21.3	49.6	91	68.1	16	50.6	115	70.1	26

(1) Load impedance for optimum P1dB efficiency.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

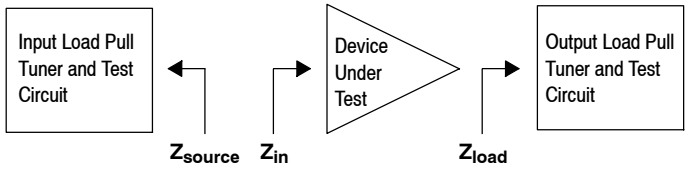


Figure 9. Carrier Side Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 28 Vdc, V_{GSB} = 1.7 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Max Linear Gain (dB)	Max Output Power							
					P1dB				P3dB			
					(dBm)	(W)	η_D (%)	AM/PM (°)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	0.88 - j3.59	0.97 + j3.83	1.35 - j4.28	15.1	54.8	302	57.0	29	54.9	309	64.7	39
1840	1.07 - j3.87	1.25 + j4.16	1.37 - j4.53	15.0	54.7	295	55.3	29	55.2	331	61.4	38
1880	1.66 - j4.15	1.80 + j4.58	1.56 - j4.77	15.1	54.6	288	55.6	28	55.3	339	58.8	36

(1) Load impedance for optimum P1dB power.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

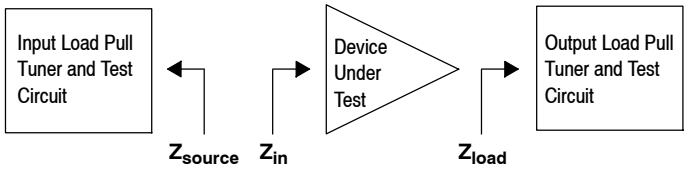


Figure 10. Peaking Side Load Pull Performance — Maximum P1dB Tuning

V_{DD} = 28 Vdc, V_{GSB} = 1.7 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Max Linear Gain (dB)	Max Drain Efficiency							
					P1dB				P3dB			
					(dBm)	(W)	η_D (%)	AM/PM (°)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	0.88 - j3.59	0.86 + j3.78	2.24 - j2.33	16.7	52.4	174	72.4	36	53.2	209	72.0	45
1840	1.07 - j3.87	1.10 + j4.10	2.05 - j2.42	16.8	52.3	170	71.6	37	53.2	209	71.0	46
1880	1.66 - j4.15	1.59 + j4.49	2.08 - j2.52	16.6	52.1	162	70.4	36	53.1	204	70.0	44

(1) Load impedance for optimum P1dB efficiency.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

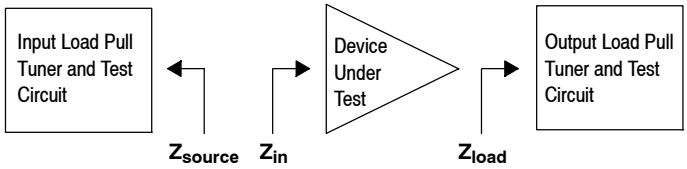


Figure 11. Peaking Side Load Pull Performance — Maximum Drain Efficiency Tuning

P1dB - TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 1840 MHz

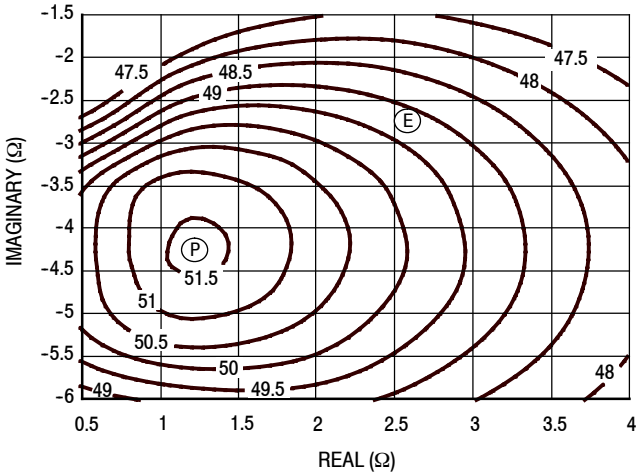


Figure 12. P1dB Load Pull Output Power Contours (dBm)

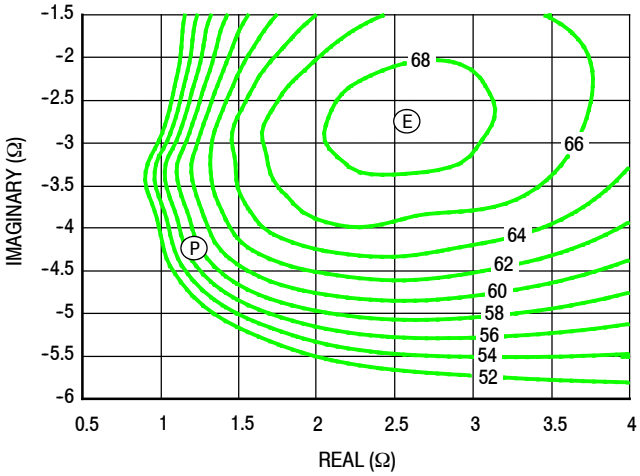


Figure 13. P1dB Load Pull Efficiency Contours (%)

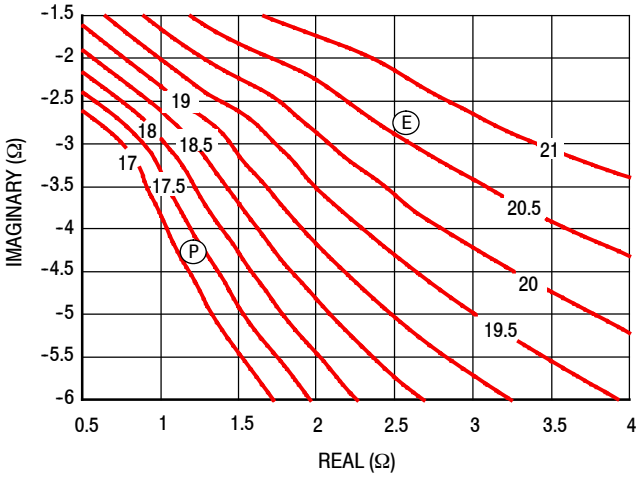


Figure 14. P1dB Load Pull Gain Contours (dB)

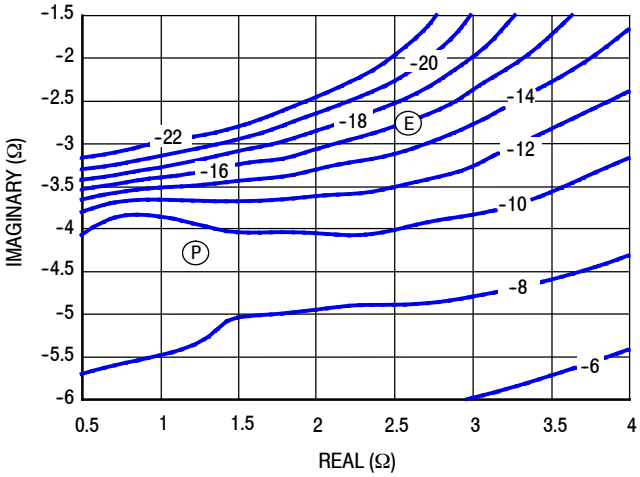


Figure 15. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Power Gain

Drain Efficiency

Linearity

Output Power

P3dB - TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 1840 MHz

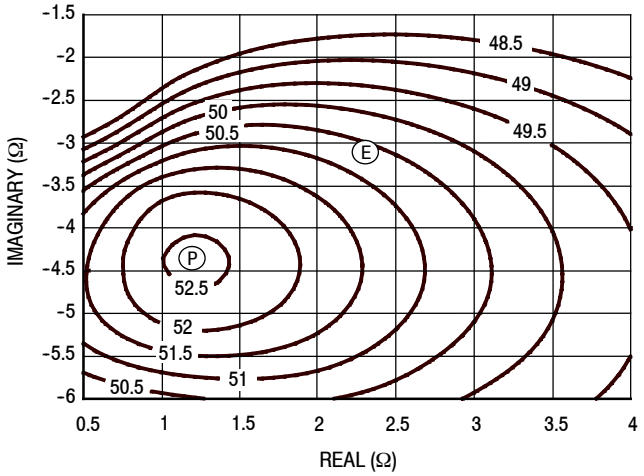


Figure 16. P3dB Load Pull Output Power Contours (dBm)

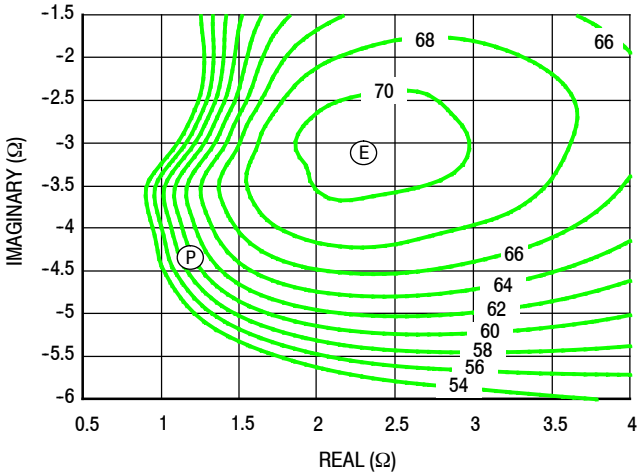


Figure 17. P3dB Load Pull Efficiency Contours (%)

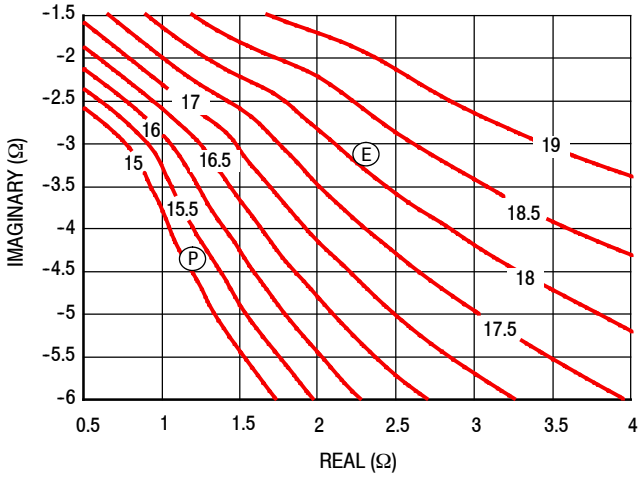


Figure 18. P3dB Load Pull Gain Contours (dB)

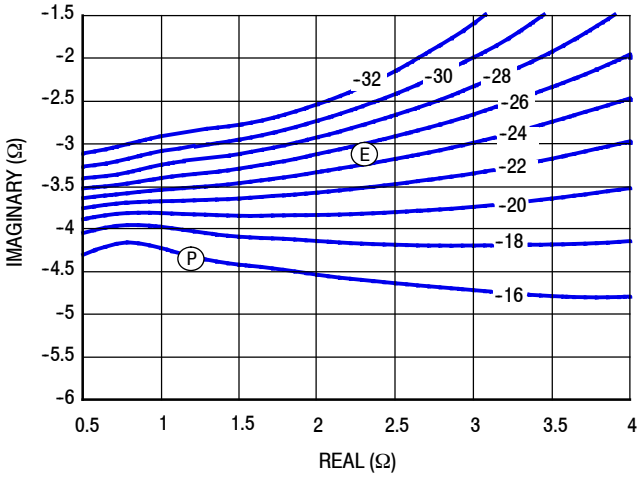


Figure 19. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Power Gain

Drain Efficiency

Linearity

Output Power

P1dB - TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 1840 MHz

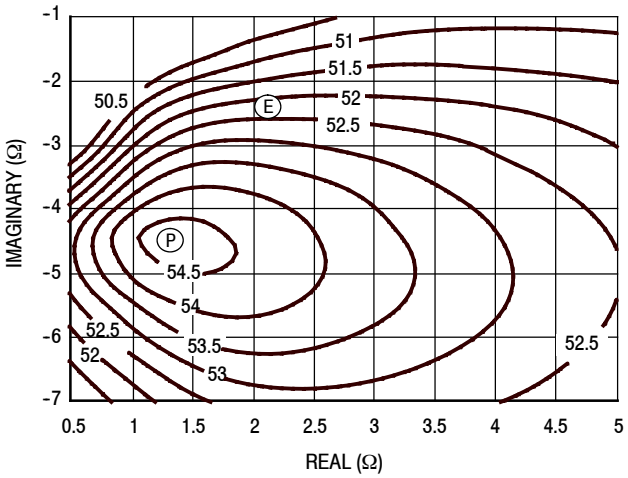


Figure 20. P1dB Load Pull Output Power Contours (dBm)

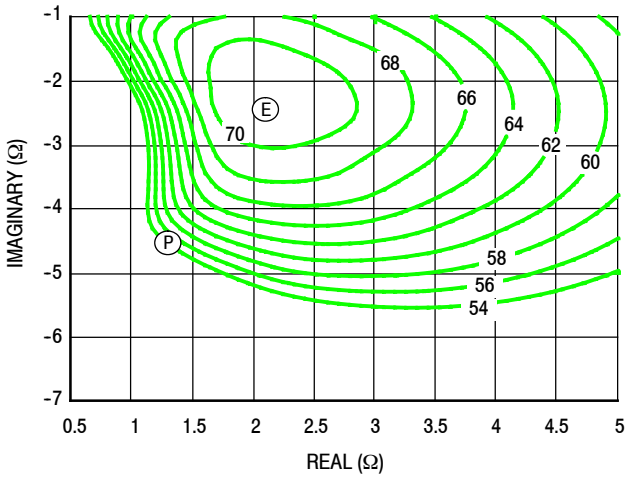


Figure 21. P1dB Load Pull Efficiency Contours (%)

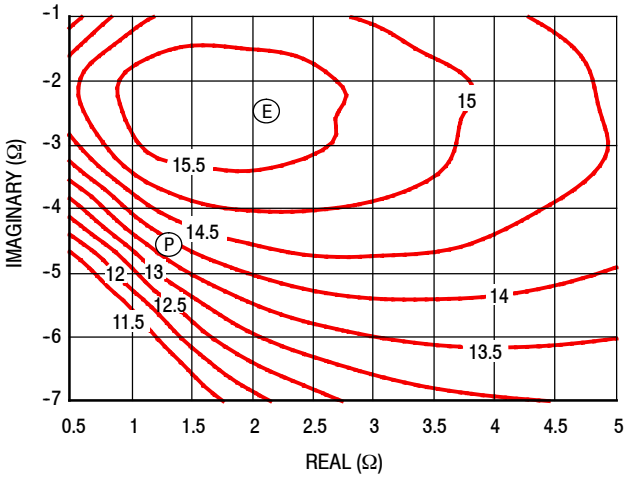


Figure 22. P1dB Load Pull Gain Contours (dB)

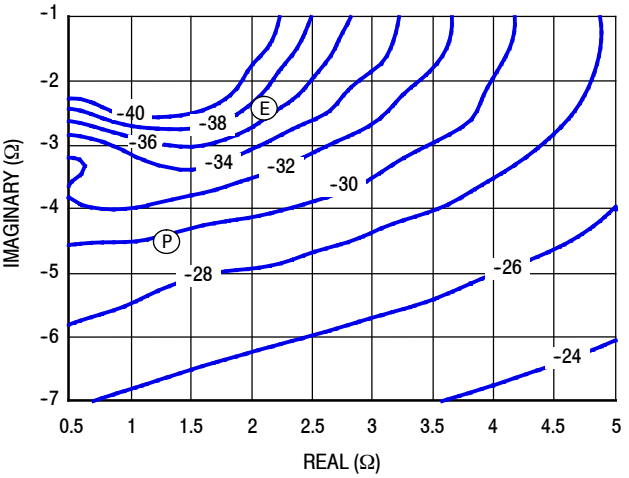


Figure 23. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Power Gain

Drain Efficiency

Linearity

Output Power

P3dB - TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 1840 MHz

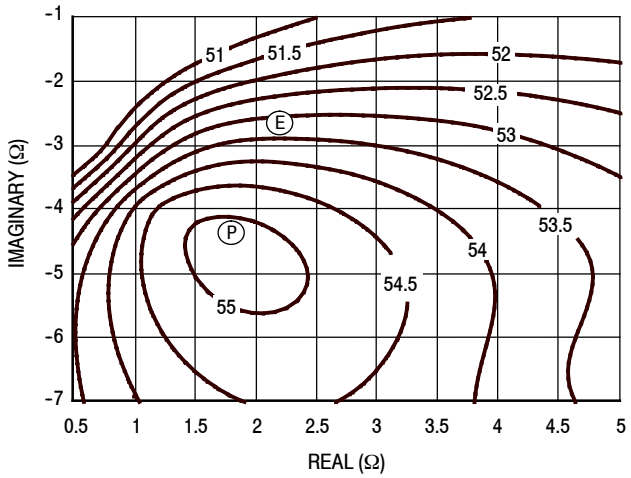


Figure 24. P3dB Load Pull Output Power Contours (dBm)

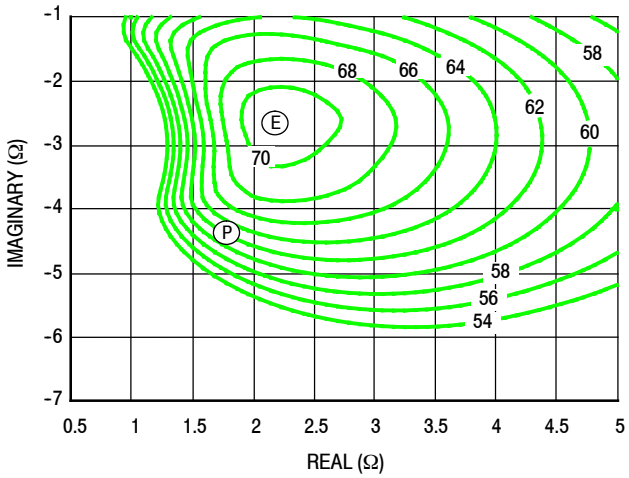


Figure 25. P3dB Load Pull Efficiency Contours (%)

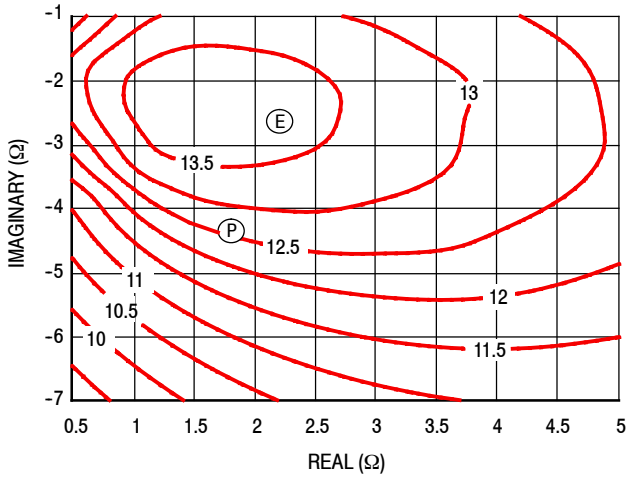


Figure 26. P3dB Load Pull Gain Contours (dB)

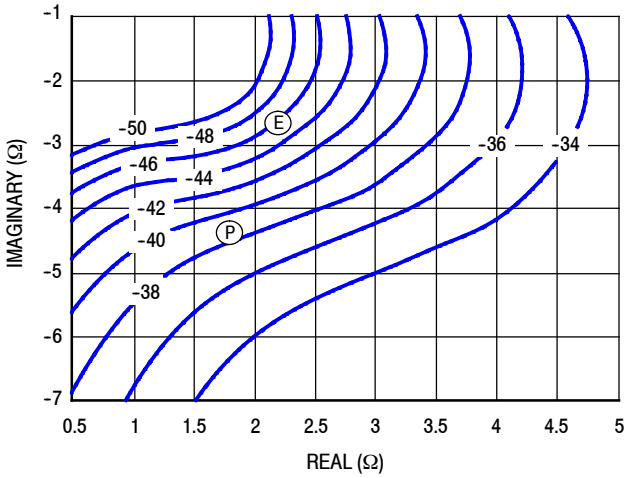


Figure 27. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

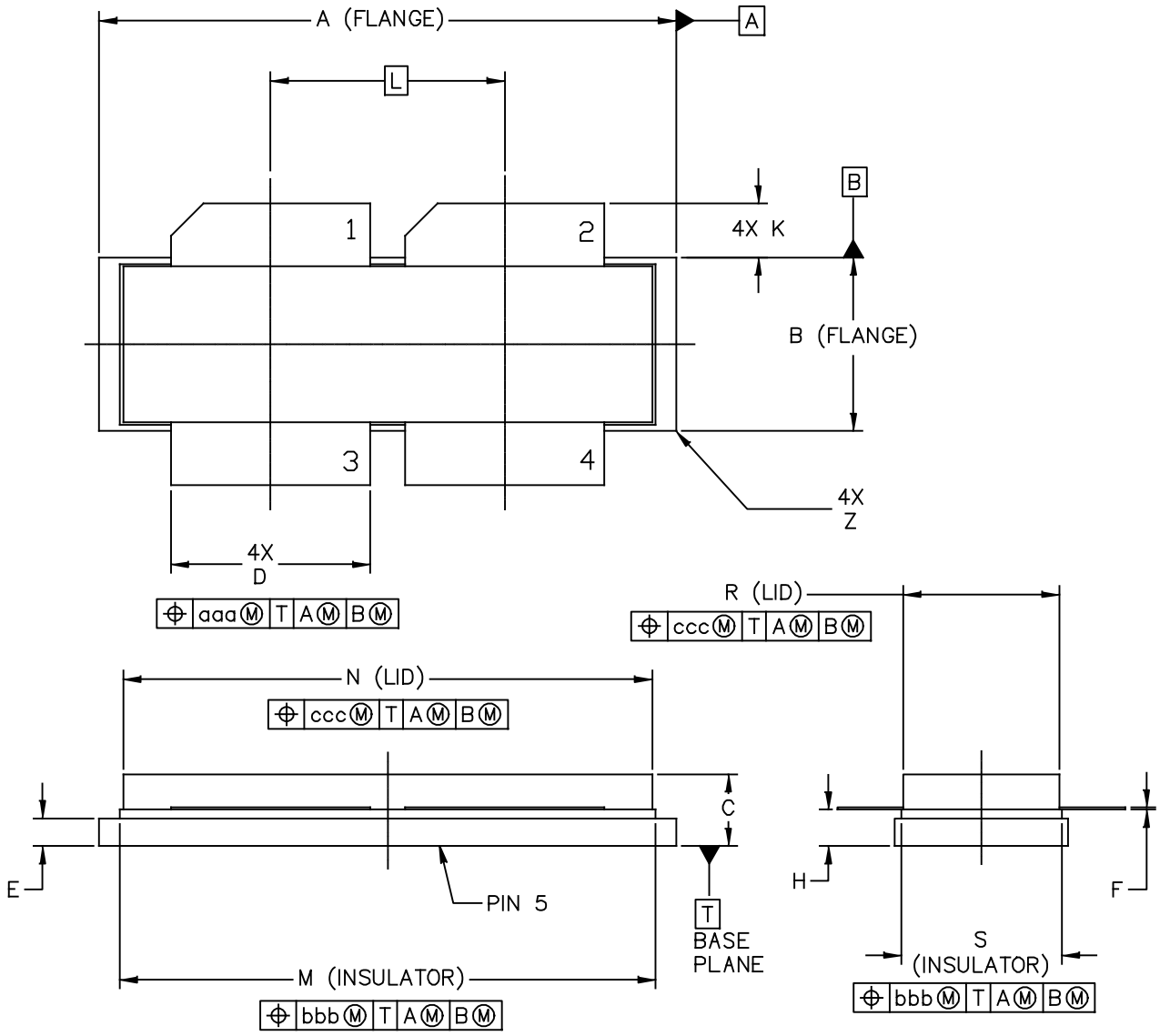
Power Gain

Drain Efficiency

Linearity

Output Power

PACKAGE DIMENSIONS



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	CASE NUMBER: 375E–04	05 AUG 2005
	STANDARD: NON–JEDEC	

NOTES:

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

2. CONTROLLING DIMENSION: INCH

3. DIMENSION H IS MEASURED .030 AWAY FROM PACKAGE BODY

STYLE 1:
PIN 1 – DRAIN
2 – DRAIN
3 – GATE
4 – GATE
5 – SOURCE

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.265	1.275	32.13	32.38	R	.355	.365	9.01	9.27
B	.395	.405	10.03	10.29	S	.365	.375	9.27	9.53
C	.150	.200	3.81	5.08	Z	---	.040	---	1.02
D	.455	.465	11.56	11.81					
E	.062	.066	1.57	1.68	aaa	.013		0.33	
F	.004	.007	0.1	0.18	bbb	.010		0.25	
H	.082	.090	2.08	2.29	ccc	.020		0.51	
K	.117	.137	2.97	3.48					
L	.540 BSC		13.72 BSC						
M	1.219	1.241	30.96	31.52					
N	1.218	1.242	30.94	31.55					

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PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following documents, software and tools to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

R5 TAPE AND REEL OPTION

The R5 tape and reel option for AFT18HW355S part will be available for 2 years after release of AFT18HW355S. Freescale Semiconductor, Inc. reserves the right to limit the quantities that will be delivered in the R5 tape and reel option. At the end of the 2 year period customers who have purchased this device in the R5 tape and reel option will be offered AFT18HW355S in the R6 tape and reel option.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Jan. 2013	• Initial Release of Data Sheet
1	Jan. 2013	• Typical Performance frequency table: updated values to show statistical broadband performance, p. 1 • Maximum Ratings table: added CW operation showing 25°C maximum CW rating limitation, p. 2 • Functional Tests table: updated typical values to reflect 1880 MHz typical performance values from p. 1 Typical Performance frequency table, changed Power Gain minimum value from 42.0% to 45.0%, p. 3 • Load Mismatch table: updated VSWR output power rating to a higher 2-carrier W-CDMA value, p. 3 • Typical Performance table: added footnote 5 to align with data in table, p. 3 • Fig. 10, Peaking Side Load Pull Performance — Maximum P1dB Tuning: corrected V_{GSB} from 1.45 Vdc to 1.7 Vdc, p. 8 • Fig. 11, Peaking Side Load Pull Performance — Maximum Drain Efficiency Tuning: corrected V_{GSB} from 1.45 Vdc to 1.7 Vdc, p. 8

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