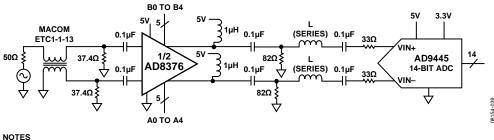# ANALOG DEVICES

AN-1408
APPLICATION NOTE

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

Using the AD8376 VGA to Drive Wide Bandwidth ADCs for High IF AC-Coupled Applications

CIRCUIT FUNCTION AND BENEFITS

The circuit described in this application note provides high performance, high frequency sampling using the AD8376, a dual channel, digitally controlled, programmable, ultralow distortion, high output linearity, variable gain amplifier (VGA), and high speed analog-to-digital converter (ADC). The AD8376 is optimized for driving high frequency intermediate frequency (IF) sampling ADCs. When coupled with an Analog Devices, Inc., high speed ADC like the AD9445 or AD9246, it provides exceptional spurious-free dynamic range (SFDR) performance beyond 100 MSPS at its maximum gain.

NOTES
1. ALL PINS AND CONNECTIONS TO AD8376 AND AD9445 NOT SHOWN.
   CONSULT PRODUCT DATA SHEETS FOR DETAILED INFORMATION.

Figure 1. Wideband ADC Interfacing Example Featuring the AD8376 and the AD9445

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CIRCUIT DESCRIPTION

This circuit employs the AD8376 VGA to provide variable gain, isolation, and source matching to a high speed ADC like the AD9445. Using this circuit with the AD8376 in a gain of 20 dB (maximum gain), an SFDR performance of 86 dBc is achieved at 100 MHz, as indicated in Figure 2.
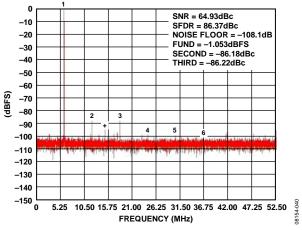

Figure 2. Measured Single-Tone Performance of the Circuit in Figure 1 for a 100 MHz Input Signal and a Sampling Rate of 105 MSPS

The AD8376 VGA is driven differentially (for optimal performance) by a wideband 1:1 transmission line balun (or impedance transformer) followed by two 37.4 Ω resistors in parallel with the 150 Ω input impedance of the AD8376. This provides a wideband match to a 50 Ω source as depicted in Figure 1. The open-collector outputs of the AD8376 are biased through the two 1 µH inductors and are ac-coupled to the two 82 Ω load resistors. The 82 Ω load resistors in parallel with the series terminated ADC impedance yields the target 150 Ω differential load impedance, which is recommended to provide the specified gain accuracy of the AD8376. The load resistors are ac-coupled from the AD9445 to avoid common-mode dc loading. The 33 Ω series resistors help to improve the isolation between the AD8376 and any switching currents present at the analog-to-digital sample-and-hold input circuitry.

The output third-order intercept point (IP3) and noise floor of the AD8376 essentially remain constant over the 24 dB available gain range. This feature is valuable in a variable gain receiver where it is desirable to maintain a constant instantaneous dynamic range as the receiver gain is modified. The output noise density is typically around 20 nV/√Hz, which is comparable with 14-bit to 16-bit sensitivity limits. The two-tone IP3 performance of the AD8376 is typically around 50 dBm. This value results in SFDR levels of better than 86 dBc when driving the AD9445, a 14-bit, 105 MSPS/125 MSPS analog-to-digital converter, up to 140 MHz input frequency. There are several configuration options available to the designer when using the AD8376. The open-collector output provides the capability of driving a variety of loads. Figure 1 shows a simplified wideband interface with the AD8376 driving an AD9445. The AD9445 is a 14-bit, 125 MSPS analog-to-digital converter with a buffered wideband input, which presents a

2 kΩ‖3 pF differential load impedance and requires a 2 V p-p differential input swing to reach full scale. The addition of the series inductors, L (series) in Figure 1, extends the bandwidth of the system and provides response flatness. Using 100 nH inductors as L (series), the wideband system response of Figure 3 is obtained. The wideband frequency response is an advantage in broadband applications such as predistortion receiver designs and instrumentation applications. However, by designing for a wide analog input frequency range, the cascaded signal-to-noise ratio (SNR) performance is somewhat degraded due to high frequency noise aliasing into the wanted Nyquist zone.
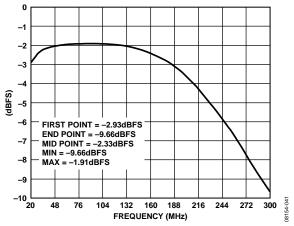

Figure 3. Measured Frequency Response of Wideband Circuit in Figure 1

COMMON VARIATIONS

An alternative narrow-band approach is presented in Figure 4. By designing a narrow band-pass antialiasing filter between the AD8376 and the target ADC, the output noise of the AD8376 outside of the intended Nyquist zone can be attenuated, helping to preserve the available SNR of the ADC.

In general, the SNR improves by several decibels when including a reasonable order antialiasing filter. For example, a low loss 1:3 (impedance ratio) input transformer is used to match the balanced input (150 Ω) to an unbalanced source (50 Ω) of the AD8376, resulting in minimum insertion loss at the input.

The narrow-band circuit shown in Figure 4 is optimized for driving some of Analog Devices popular unbuffered input ADCs, such as the AD9246, AD9640, and AD6655. Table 1 includes antialiasing filter component recommendations for popular IF sampling center frequencies. Inductor L5 works in parallel with the on-chip ADC input capacitance and a portion of the capacitance presented by C4 to form a resonant tank circuit. The resonant tank helps to ensure the ADC input looks like a real resistance at the target center frequency. Additionally, the L5 inductor shorts the ADC inputs at dc, which introduces a zero into the transfer function. The 1 nF ac coupling capacitors and the 1 µH bias chokes introduce additional zeros into the transfer function. The final overall frequency response takes on a band-pass characteristic, helping to reject noise outside of the intended Nyquist zone. Table 1 provides initial suggestions for prototyping purposes. Some empirical optimization may be

needed to help compensate for actual printed circuit boards (PCB) parasitics. Details of designing the interstage filters can be found in the References section.

The circuit in Figure 1 requires 1% resistors for the two 37.4 Ω values (1/10 W). Other resistors can be 10% (1/10 W). Capacitors must be 10% ceramic chips. The circuit in Figure 4 requires 1% resistors for the two 165 Ω values (1/10 W). Other resistors, capacitors, and inductors can be 10% values.

Excellent layout, grounding, and decoupling techniques must be utilized to achieve the desired performance from the circuits discussed in this application note. At a minimum, a 4-layer PCB must be used with one ground plane layer, one power plane layer, and two signal layers.
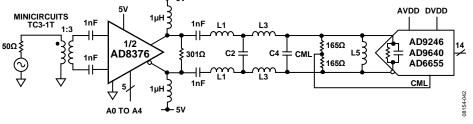
All IC power pins must be decoupled to the ground plane with low inductance multilayer ceramic capacitors (MLCC) of 0.01 μF to 0.1 μF (this is not shown in the diagrams for simplicity). Follow the recommendations on the individual data sheets for the AD8376, AD9246, and AD9445.

The AD8376, AD9246, and AD9445 product evaluation boards need to be consulted for recommended layout and critical component placement. These can be accessed through the main product pages for the devices.

The A0 to A4 and B0 to B4 digital inputs, ENBA, and ENBB must not be more than 0.6 V more positive than the AD8376 power supply or more than 0.6 V below ground to prevent damaging the internal electrostatic discharge (ESD) protection diodes of the AD8376. Damage does not occur if the power to the logic driving the AD8376 is derived from the same power supply that powers the AD8376. The AD8376 is not susceptible to latch-up because it is manufactured on a bipolar process.

Even though the AD8376 and the AD9445 (or other ADC) may be powered from different supplies, sequencing is not an issue because the input signal to the ADC is ac-coupled.

The individual data sheet for the ADC needs to be consulted regarding the proper sequencing of the AVDD and the DVDD power supplies (if separate supplies are used).

NOTES
1. ALL PINS AND CONNECTIONS TO AD8376 AND AD9445 NOT SHOWN. CONSULT PRODUCT DATA SHEETS FOR DETAILED INFORMATION.

Figure 4. Narrow-Band IF Sampling Solution for Unbuffered Switched Capacitor ADC Inputs

Table 1. Interface Filter Recommendations for Various IF Sampling Frequencies

Center Frequency (MHz)	1 dB Bandwidth (MHz)	L1 (nH)	C2 (pF)	L3 (nH)	C4 (pF)	L5 (nH)
96	27	390	5.6	390	22	100
140	30	330	3.3	330	20	56
170	32	270	2.7	270	20	39
211	32	220	2.2	220	18	27

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