

<b>PCN Number:</b>	20190221000.1		<b>PCN Date:</b>	Feb 27, 2019
<b>Title:</b>	Design Change of Select Devices			
<b>Customer Contact:</b>	<a href="#">PCN Manager</a>		<b>Dept:</b>	Quality Services
<b>Proposed 1<sup>st</sup> Ship Date:</b>	May 27, 2019	<b>Estimated Sample Availability:</b>	Date provided at sample request.	
<b>Change Type:</b>				
<input type="checkbox"/>	Assembly Site	<input type="checkbox"/>	Assembly Process	<input type="checkbox"/>
<input checked="" type="checkbox"/>	Design	<input type="checkbox"/>	Electrical Specification	<input type="checkbox"/>
<input type="checkbox"/>	Test Site	<input type="checkbox"/>	Packing/Shipping/Labeling	<input type="checkbox"/>
<input type="checkbox"/>	Wafer Bump Site	<input type="checkbox"/>	Wafer Bump Material	<input type="checkbox"/>
<input type="checkbox"/>	Wafer Fab Site	<input type="checkbox"/>	Wafer Fab Materials	<input type="checkbox"/>
<input type="checkbox"/>		<input type="checkbox"/>	Part number change	
<b>PCN Details</b>				
<b>Description of Change:</b>				
<p>This notification is to inform of a design change to TPS65903x family of devices. The design change is a metal change that will remove the POR (power on reset) constraints and improve the LDO1 and LDO2 functionality.</p> <p>With previous silicon revisions, a POR could not be reliably generated in the following conditions:</p> <ol style="list-style-type: none"> <li>VCC1 falling slew rate below 2.0V is faster than 90 mV/ms</li> <li>VCC1 (Input power to the device) is turned off then turned back on after a short delay</li> </ol> <p>New silicon will allow these conditions to still generate a proper POR.</p> <p>New silicon will also fix LDO1 and LDO2 occurrence where they get stuck off when VCC1 drops below VSYS_LO and POR.</p> <p>The device revision register (DESIGNREV) will reflect the change in silicon by changing contents from 0x3 to 0x4. There is no change in part number or top side marking.</p> <p>The register map can be found here: <a href="http://www.ti.com/lit/pdf/sliu015">http://www.ti.com/lit/pdf/sliu015</a></p> <p><b>Note: The silicon updates do not require system design changes.</b></p> <p>Affected devices are listed in the Product Affected section of this document.</p>				
<b>Reason for Change:</b>				
Remove POR generation restrictions and allow LDO1 and LDO2 to reliably turn on when VCC1 drops between VSYS_LO and POR.				
<b>Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative):</b>				
None				
<b>Product Affected:</b>				
TPS6590376ZWSR	TPS6590377ZWST	TPS6590379ZWSR	TPS659037A394ZWSR	
TPS6590376ZWST	TPS6590378ZWSR	TPS6590379ZWST	TPS659037A398ZWSR	
TPS6590377ZWSR	TPS6590378ZWST	TPS659037A38CZWSR	TPS659037A399ZWSR	

## Qualification Report

### Approve Date 4-Feb-2019

#### Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	Test Name / Condition	Duration	Qual Device: TPS6590371ZW SR	QBS Product: TPS659039XXIZWS RQ1	QBS Product: TPS659039XXIZWS RQ1	QBS Product: TPS659039XXIZW SRQ1
THB	85C/85%RH	1000 Hrs	-	-	1/77/0	2/154/0
uHAST	Unbiased HAST, 110C/85%RH	264 Hours	-	-	1/77/0	2/154/0
TC	Temperature Cycle - 65/150C	1000 Cycles	-	-	1/77/0	2/154/0
HTSL	High Temp Storage Bake 150C	500 Hours	-	-	1/45/0	1/45/0
HTOL	Life Test, 125C	1000 Hours	-	-	1/77/0	2/154/0
WBP	Bond Pull	Wires	-	-	1/30/0	1/30/0
WBS	Ball Bond Shear	Wires	-	-	1/30/0	1/30/0
CDM	ESD - CDM	750 V (all pins)	-	1/3/0 (MIHO and RFAB each)	1/3/0	1/3/0
		250V (all pins)	1/3/0	-	-	-
HBM	ESD - HBM	2000 V	-	1/3/0 (MIHO and RFAB each)	1/3/0	1/3/0
PD	Physical Dimensions	-	-	-	1/10/0	2/20/0
ED	Electrical Characterization	Per Datasheet Parameters	-	Pass	Pass	Pass
LU	Latch-up	( Per JESD78 )	-	1/6/0  at 105C I2C and SPI balls, 90 mA LDOVANA_OUT, -60 mA All other balls, 100 mA (MIHO and RFAB each)	1/6/0  at 105C I2C and SPI balls, 90 mA LDOVANA_OUT, -60 mA All other balls, 100 mA	1/6/0  at 105C I2C and SPI balls, 90 mA LDOVANA_OUT, -60 mA All other balls, 100 mA

- Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
- The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
- The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours
- The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Quality and Environmental data is available at TI's external Web site: <http://www.ti.com/>

#### Green/Pb-free Status:

Qualified Pb-Free(SMT) and Green

For questions regarding this notice, e-mails can be sent to the regional contacts shown below, or you can contact your local Field Sales Representative.

<b>Location</b>	<b>E-Mail</b>
USA	<a href="mailto:PCNAmericasContact@list.ti.com">PCNAmericasContact@list.ti.com</a>
Europe	<a href="mailto:PCNEuropeContact@list.ti.com">PCNEuropeContact@list.ti.com</a>
Asia Pacific	<a href="mailto:PCNAsiaContact@list.ti.com">PCNAsiaContact@list.ti.com</a>
WW PCN Team	<a href="mailto:PCN_ww_admin_team@list.ti.com">PCN_ww_admin_team@list.ti.com</a>