PCN Number:	20190222000.0	PCN Date:	February 28, 2019
Title:	Datasheet for TPS65917-Q1 and TPS65919-Q1		
Customer Contact:	PCN Manager	Dept:	Quality Services

Change Type:

☐	Assembly Site	☐	Design	☐	Wafer Bump Site
☐	Assembly Process	☒	Data Sheet	☐	Wafer Bump Material
☐	Assembly Materials	☐	Part number change	☐	Wafer Bump Process
☐	Mechanical Specification	☐	Test Site	☐	Wafer Fab Site
☐	Packing/Shipping/Labeling	☐	Test Process	☐	Wafer Fab Materials
				☐	Wafer Fab Process

Notification Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification.
The product datasheet(s) is being updated as summarized below.
The following change history provides further details.

TEXAS INSTRUMENTS

TPS65917-Q1

SLVSCO4D – JULY 2015 – REVISED FEBRUARY 2019

Changes from Revision C (March 2017) to Revision D — **Page**

- Added footnote recommending not to pull open-drain GPIOs up to an always-on voltage domain 9
- Clarified that LDO1 and LDO2 input pins are not included in this minimum recommended operating voltage. See *Electrical Characteristics: LDO Regulators* for more information. 12
- Added LDO and SMPS output capacitance footnote 13
- Added SMPS Output voltage slew rate description 15
- Changed the comparison condition from VCCA to VCC_SENSE in the *Embedded Power Controller* section 32
- Added typical debounce time from POWERHOLD to the enable of the first rail in the power sequence. 33
- Changed discharge resistance to match electrical characteristics table 42
- Changed description of clock dithering from internal to external only 44
- Added information about shutdown timing during short circuit detection 45
- Updated POWERGOOD block diagram and description to clarify dual phase operation. 46
- Added notes to the *SMPS Controls for DVS* image 48
- Added the equation to convert GPADC code to internal die temperature in the *12-Bit Sigma-Delta General-Purpose ADC (GPADC)* section 52
- Additional description of VSYS_LO functionality 66
- Added details on identifying device version. 69
- SMPS and LDO output capacitance specification further explained 74
- Added design considerations for VCCA capacitance to support loss of power 74
- Corrected 9-Vpp with 7V absolute maximum specification in the *Layout Guidelines* section 79
- Updated requirements relating to measurement of high-side and low-side FETs in the *Layout Guidelines* section 80
- Updated images and description on differential measurements across high-side and low-side FETs 81

TEXAS INSTRUMENTS

TPS65919-Q1

SLVSDM1A – AUGUST 2017 – REVISED FEBRUARY 2019

Changes from Original (August 2017) to Revision A — **Page**

- Clarified that LDO1 and LDO2 input pins are not included in this minimum recommended operating voltage. See *Electrical Characteristics: LDO Regulators* for more information. 12
- Added LDO and SMPS output capacitance footnote 13
- Added SMPS Output voltage slew rate description 15
- Changed the comparison condition from VCCA to VCC_SENSE in the *Embedded Power Controller* section 31

- Added typical debounce time from POWERHOLD to the enable of the first rail in the power sequence. 32
- Changed discharge resistance to match electrical characteristics table section 41
- Changed description of clock dithering from internal to external only..... 43
- Added information about shutdown timing during short circuit detection 44
- Updated POWERGOOD block diagram and description to clarify dual phase operation. 44
- Added notes to the *SMPS Controls for DVS* image 46
- Added the equation to convert GPADC code to internal die temperature in the *12-Bit Sigma-Delta General-Purpose ADC (GPADC)* section..... 50
- Additional description of VSYS_LO functionality 64
- Added details on identifying device version. 67
- SMPS and LDO output capacitance specification further explained 72
- Added design considerations for VCCA capacitance to support loss of power..... 72
- Corrected 9-Vpp with 7V absolute maximum specification in the *Layout Guidelines* section..... 77
- Updated requirements relating to measurement of high-side and low-side FETs in the *Layout Guidelines* section... 78
- Updated images and description on differential measurements across high-side and low-side FETs 79

The datasheet number will be changing.

Device Family	Change From:	Change To:
TPS65917-Q1	SLVSCO4C	SLVSCO4D
TPS65919-Q1	SLVSDM1	SLVSDM1A

These changes may be reviewed at the datasheet links provided.

http://www.ti.com/product/TPS65917-Q1

http://www.ti.com/product/TPS65919-Q1

Reason for Change:

To accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.

Changes to product identification resulting from this PCN:

None.

Product Affected:

O917A11CTRGZRQ1	O917A131TRGZTQ1	O917A135TRGZRQ1	O917A148TRGZRQ1
O917A123TRGZRQ1	O917A132TRGZRQ1	O917A136TRGZRQ1	O917A14DTRGZRQ1
O917A12ETRGZRQ1	O917A132TRGZTQ1	O917A139TRGZRQ1	O917A14DTRGZTQ1
O917A130TRGZRQ1	O917A133TRGZRQ1	O917A13ATRGZRQ1	O917A14FTRGZRQ1
O917A130TRGZTQ1	O917A133TRGZTQ1	O917A13BTRGZRQ1	O917A14FTRGZTQ1
O917A131TRGZRQ1	O917A134TRGZRQ1	O917A142TRGZRQ1	O917A151TRGZRQ1
O917A152TRGZRQ1	O919A14CTRGZRQ1	O919A14CTRGZTQ1	O919A14ETRGZRQ1
O917A152TRGZTQ1	O919A14ETRGZTQ1	O919A152TRGZRQ1	O919A152TRGZTQ1

For questions regarding this notice, e-mails can be sent to the contacts shown below or your local Field Sales Representative.

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