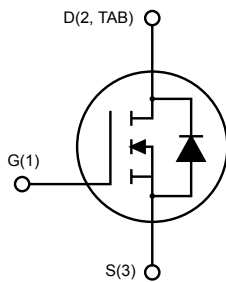
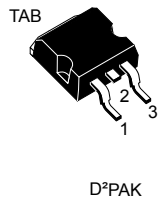


## N-channel 650 V, 95 mΩ typ., 24 A MDmesh™ M5 Power MOSFET in D<sup>2</sup>PAK package



### Features

Order codes	V <sub>DS</sub> at T <sub>jmax.</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STB32N65M5	710 V	119 mΩ	24 A

- Extremely low R<sub>DS(on)</sub>
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET based on the MDmesh™ M5 innovative vertical process technology combined with the well-known PowerMESH™ horizontal layout. The resulting product offers extremely low on-resistance, making it particularly suitable for applications requiring high power and superior efficiency.



#### Product status link

[STB32N65M5](#)

#### Product summary

<b>Order code</b>	STB32N65M5
<b>Marking</b>	32N65M5
<b>Package</b>	D <sup>2</sup> PAK
<b>Packing</b>	Tape and reel

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	24	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	15	A
$I_{DM}^{(1)}$	Drain current (pulsed)	96	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	150	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$T_j$	Operating junction temperature range	-55 to 150	$^\circ\text{C}$
$T_{stg}$	Storage temperature range		

1. Pulse width limited by safe operating area.

2.  $I_{SD} \leq 24\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DS(peak)} \leq V_{(BR)DSS}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.83	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	30	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1 inch<sup>2</sup>, 2oz Cu.

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ Max)	8	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	650	mJ

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0\text{ V}$	650			V
$I_{DSS}$	Zero gate voltage drain current	$V_{DS} = 650\text{ V}$ , $V_{GS} = 0\text{ V}$ ,			1	$\mu\text{A}$
		$V_{DS} = 650\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_C = 125\text{ °C}$ <sup>(1)</sup>			100	$\mu\text{A}$
$I_{GSS}$	Gate body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 12\text{ A}$		95	119	m $\Omega$

1. Defined by design, not subject to production test.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$		3320		pF
$C_{oss}$	Output capacitance		-	75	-	
$C_{riss}$	Reverse transfer capacitance			5		
$C_{o(tr)}$ <sup>(1)</sup>	Equivalent capacitance time related	$V_{GS} = 0\text{ V}$ , $V_{DS} = 0\text{ to }520\text{ V}$	-	210	-	pF
$C_{o(er)}$ <sup>(2)</sup>	Equivalent capacitance energy related		-	70	-	pF
$R_g$	Gate input resistance	$f = 1\text{ MHz}$ , $I_D = 0\text{ A}$	-	2	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 520\text{ V}$ , $I_D = 12\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 15. Test circuit for gate charge behavior)		72		nC
$Q_{gs}$	Gate-source charge		-	17	-	
$Q_{gd}$	Gate-drain charge			29		

1.  $C_{o(tr)}$  time related is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

2.  $C_{o(er)}$  energy related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off delay time	$V_{DD} = 400\text{ V}$ , $I_D = 15\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times and Figure 19. Switching time waveform)		53		ns
$t_r$	Rise time			12		
$t_c$	Cross time		-	29	-	
$t_f$	Fall time			16		

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
$I_{SD}$	Source-drain current		-		24	A	
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				96		
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 24\text{ A}$ , $V_{GS} = 0\text{ V}$	-		1.5	V	
$t_{rr}$	Reverse recovery time	$I_{SD} = 24\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	375		ns	
$Q_{rr}$	Reverse recovery charge			6			μC
$I_{RRM}$	Reverse recovery current			33			
$t_{rr}$	Reverse recovery time	$I_{SD} = 24\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ °C}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	440		ns	
$Q_{rr}$	Reverse recovery charge			8			μC
$I_{RRM}$	Reverse recovery current			36			

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs, duty cycle 1.5%.

## 2.1 Electrical characteristics curves

Figure 1. Safe operating area

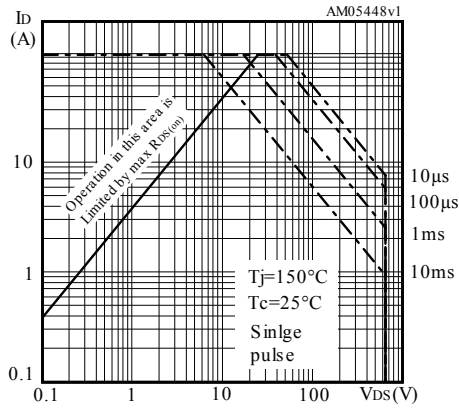


Figure 2. Thermal impedance

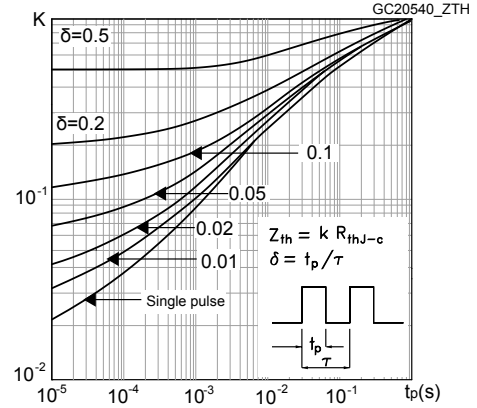


Figure 3. Output characteristics

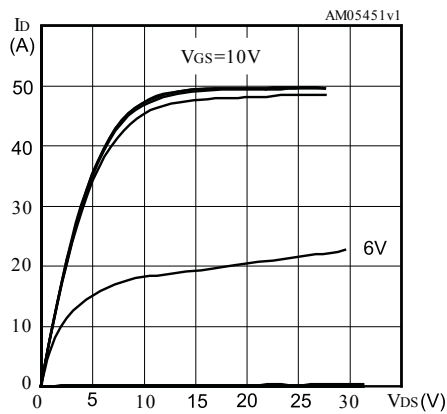


Figure 4. Transfer characteristics

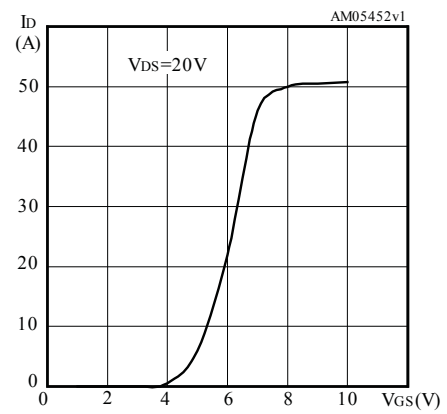


Figure 5. Gate charge vs gate-source voltage

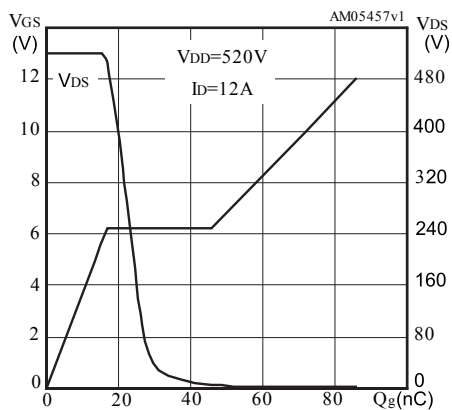


Figure 6. Static drain-source on resistance

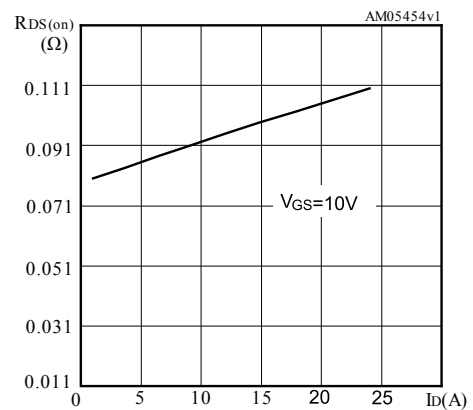


Figure 7. Capacitance variations

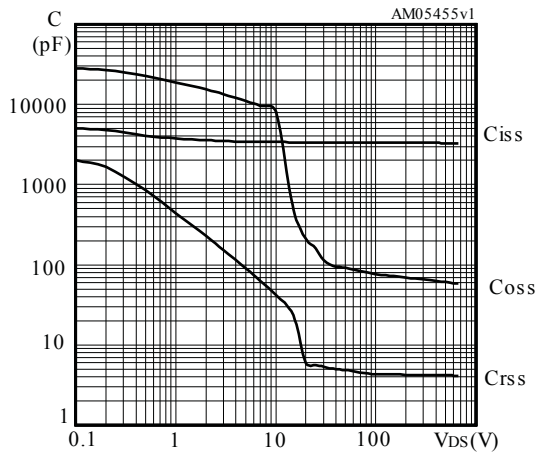


Figure 8. Output capacitance stored energy

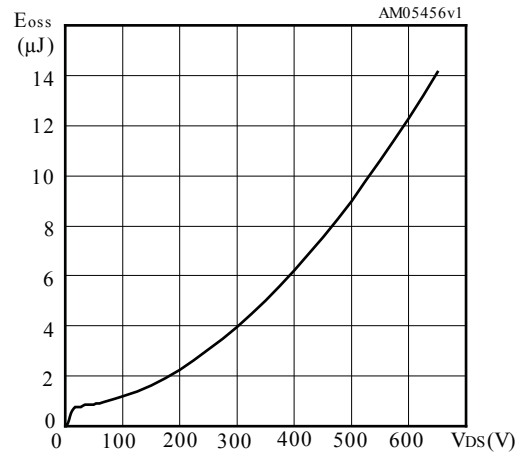


Figure 9. Normalized gate threshold voltage vs temperature

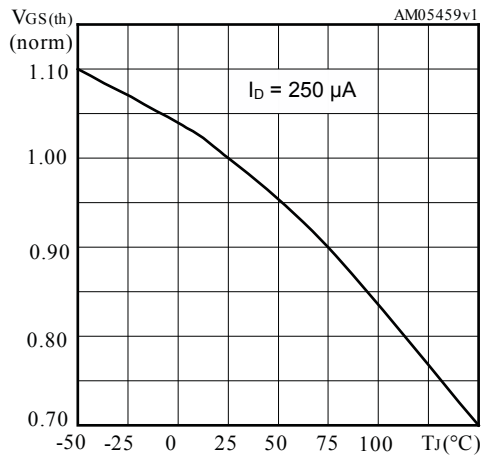


Figure 10. Normalized on resistance vs temperature

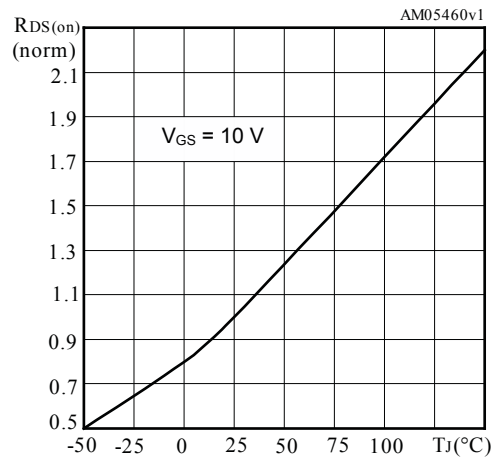


Figure 11. Source-drain diode forward characteristics

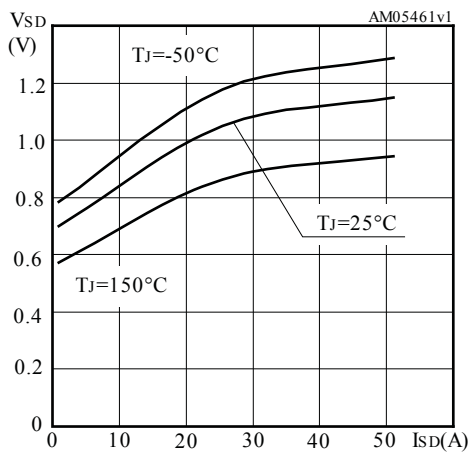


Figure 12. Normalized V<sub>(BR)DSS</sub> vs temperature

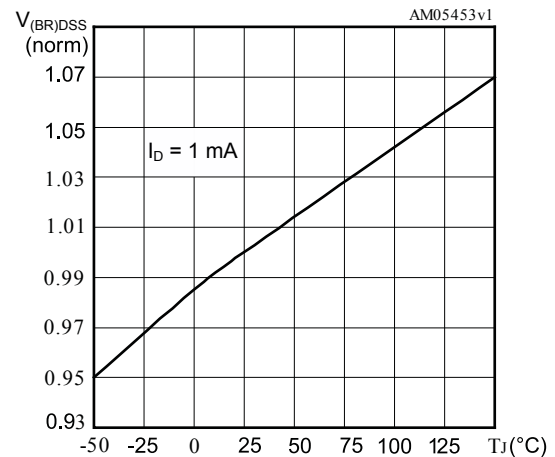
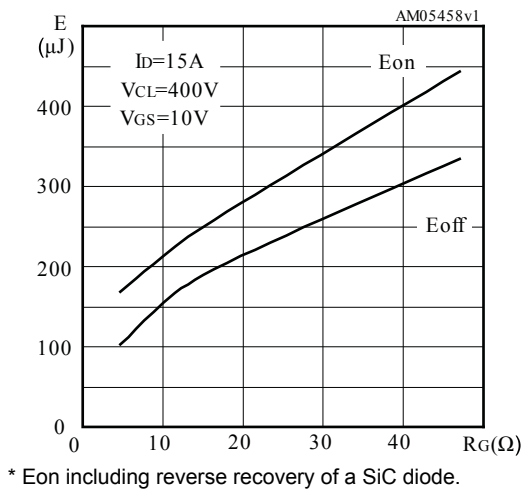
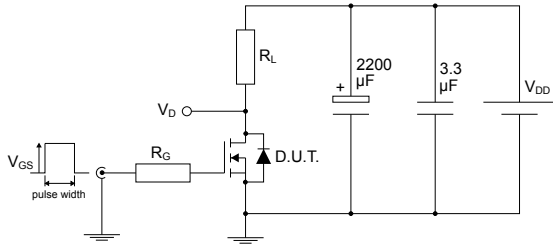


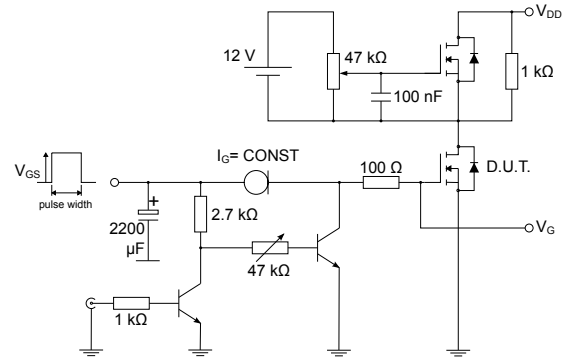
Figure 13. Switching energy vs gate resistance



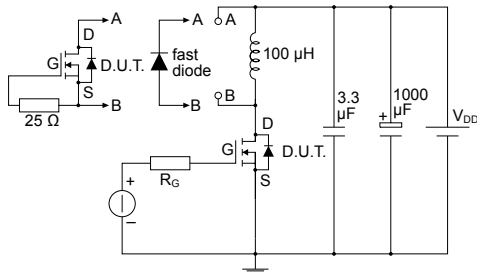
### 3 Test circuits

**Figure 14. Test circuit for resistive load switching times**


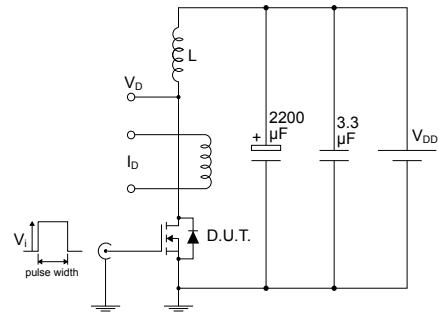
AM01488v1

**Figure 15. Test circuit for gate charge behavior**


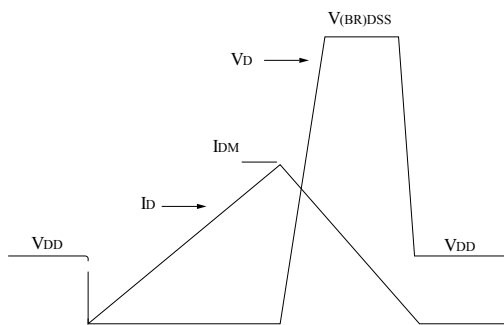
AM01469v1

**Figure 16. Test circuit for inductive load switching and diode recovery times**


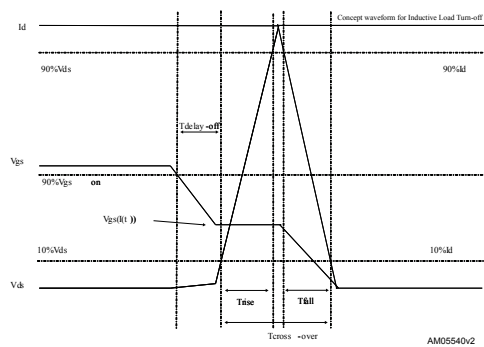
AM01470v1

**Figure 17. Unclamped inductive load test circuit**


AM01471v1

**Figure 18. Unclamped inductive waveform**


AM01472v1

**Figure 19. Switching time waveform**


AM05540v2

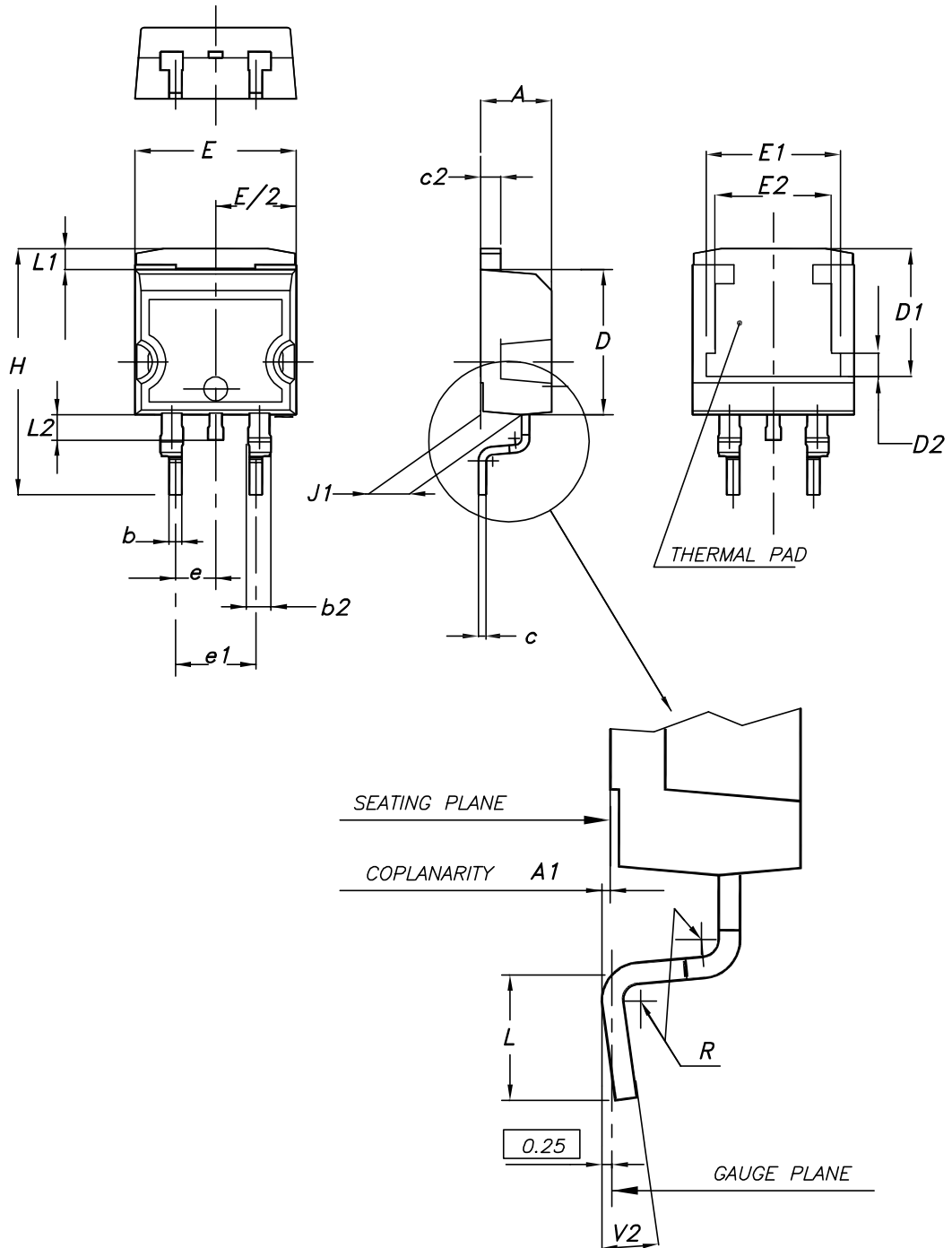


## 4 Package information

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In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK<sup>®</sup>** packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

**4.1 D<sup>2</sup>PAK (TO-263) type A package information**

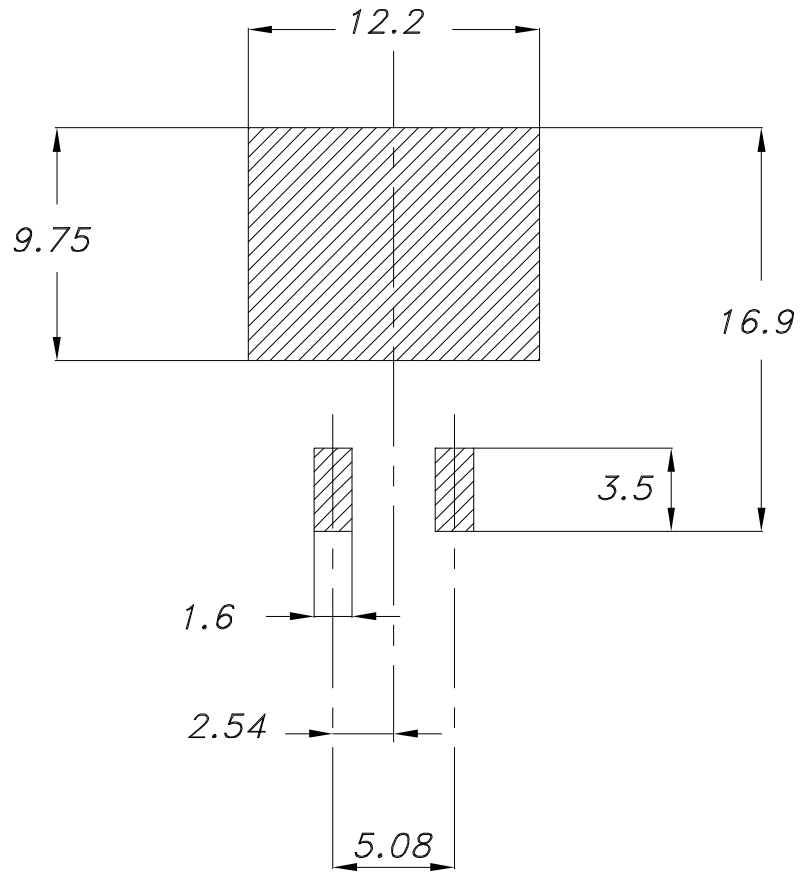
 Figure 20. D<sup>2</sup>PAK (TO-263) type A package outline


0079457\_25

**Table 8. D<sup>2</sup>PAK (TO-263) type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

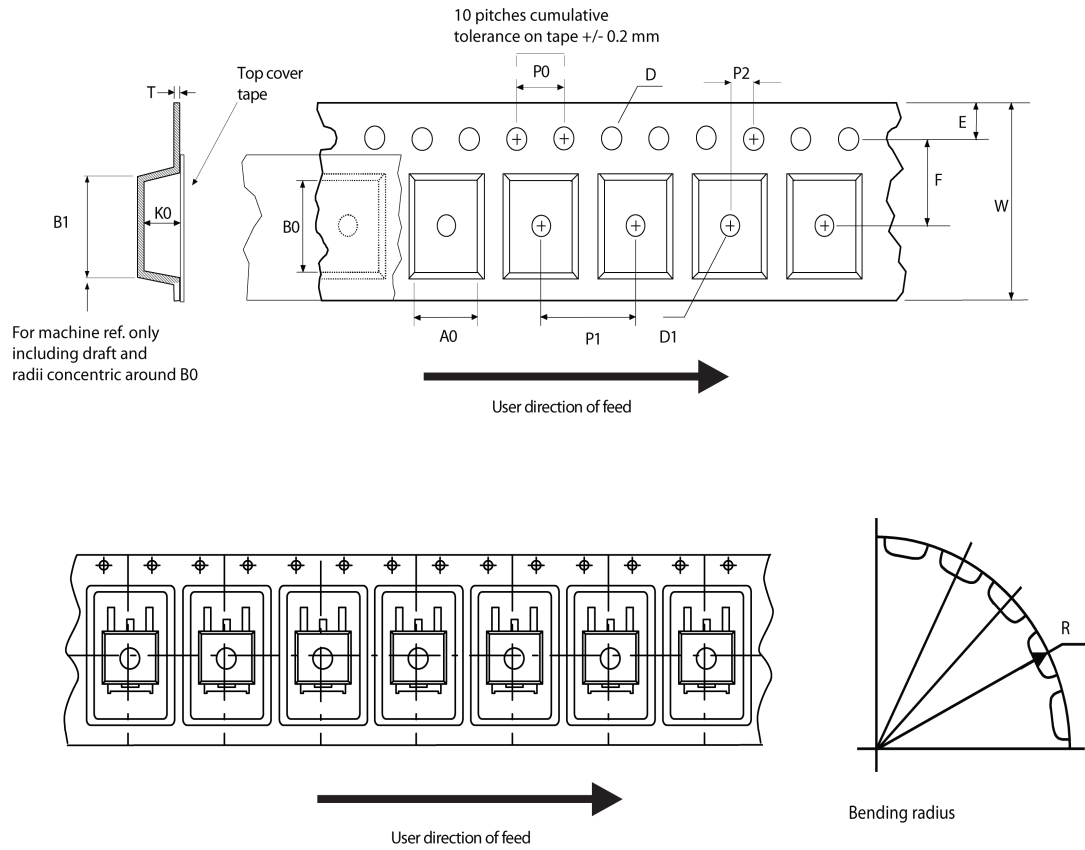
Figure 21. D<sup>2</sup>PAK (TO-263) recommended footprint (dimensions are in mm)



Footprint

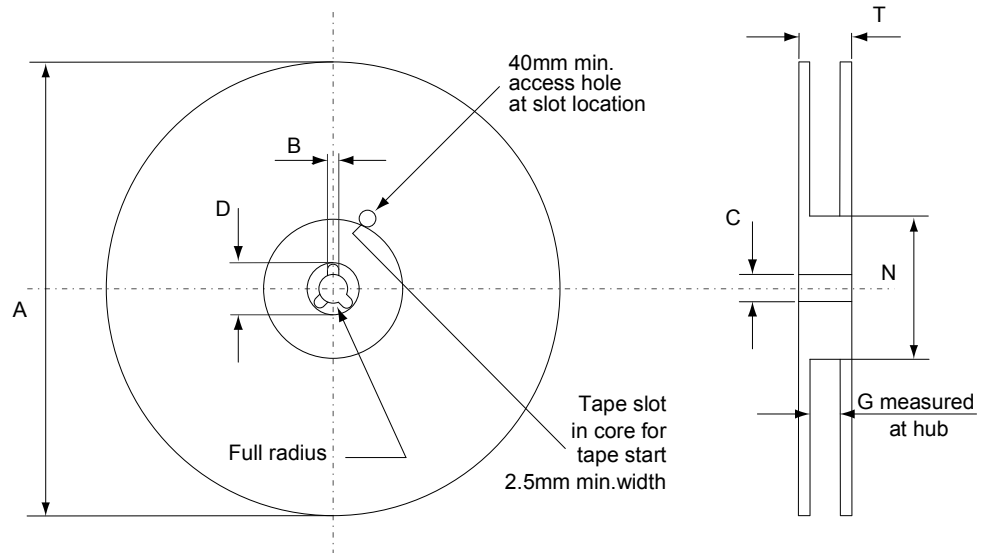
## 4.2 D<sup>2</sup>PAK packing information

Figure 22. D<sup>2</sup>PAK tape outline



AM08852v1

**Figure 23. D<sup>2</sup>PAK reel outline**



AM06038v1

**Table 9. D<sup>2</sup>PAK tape and reel mechanical data**

Tape			Reel				
Dim.	mm		Dim.	mm			
	Min.	Max.		Min.	Max.		
A0	10.5	10.7	A		330		
B0	15.7	15.9	B	1.5			
D	1.5	1.6	C	12.8	13.2		
D1	1.59	1.61	D	20.2			
E	1.65	1.85	G	24.4	26.4		
F	11.4	11.6	N	100			
K0	4.8	5.0	T		30.4		
P0	3.9	4.1	Base quantity				
P1	11.9	12.1				1000	
P2	1.9	2.1				Bulk quantity	
R	50					1000	
T	0.25	0.35					
W	23.7	24.3					

## Revision history

Table 10. Document revision history

Date	Version	Changes
16-Jan-2009	1	First release
01-Sep-2009	2	Document status promoted from preliminary data to datasheet.
30-Sep-2009	3	Corrected $V_{GS}$ value on Table 2: Absolute maximum ratings
06-Oct-2011	4	<p><math>C_{o(er)}</math> and <math>C_{o(tr)}</math> values changed in <i>Table 5: Dynamic</i></p> <p><i>Table 6: Switching times</i> parameters updates</p> <p><i>Figure 24: Switching time waveform</i> has been corrected</p> <p>Minor text changes</p> <p><i>Section 4: Package mechanical data</i> has been modified. Added:</p> <ul style="list-style-type: none"> <li>– <i>Table 8: D<sup>2</sup>PAK (TO-263) mechanical data, Figure 25: D<sup>2</sup>PAK (TO-263) drawing and Figure 26: D<sup>2</sup>PAK footprint,</i></li> <li>– <i>Table 9: TO-220FP mechanical data, and Figure 27: TO-220FP drawing;</i></li> <li>– <i>Table 10: I<sup>2</sup>PAK (TO-262) mechanical data, and Figure 28: I<sup>2</sup>PAK (TO-262) drawing;</i></li> <li>– <i>Table 11: TO-220 type A mechanical data, and Figure 29: TO-220 type A drawing;</i></li> <li>– <i>Table 12: TO-247 mechanical data, and Figure 30: TO-247 drawing;</i></li> </ul> <p><i>Section 5: Packaging mechanical data</i> has been modified. Added:</p> <ul style="list-style-type: none"> <li>– <i>Table 13: D<sup>2</sup>PAK (TO-263) tape and reel mechanical data, Figure 31: Tape and Figure 32: Reel;</i></li> </ul>
02-Nov-2018	5	<p>The part numbers STF32N65M5, STI32N65M5, STP32N65M5, STW32N65M5 have been moved to a separate datasheet.</p> <p>Content reworked to improve readability, no technical changes.</p>

## Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>2</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>3</b>
<b>2.1</b>	Electrical characteristics curves .....	<b>5</b>
<b>3</b>	<b>Test circuits</b> .....	<b>8</b>
<b>4</b>	<b>Package information</b> .....	<b>9</b>
<b>4.1</b>	D <sup>2</sup> PAK (TO-263) type A package information .....	<b>9</b>
<b>4.2</b>	D <sup>2</sup> PAK packing information .....	<b>12</b>
	<b>Revision history</b> .....	<b>15</b>



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