

## FEATURES

- Handles 10,000pF Capacitive Load
- 450 $\mu$ V Max Offset Voltage
- 1200 $\mu$ V Max Offset Voltage in S8 Package
- 50pA Bias Current at 70°C
- 13nV/ $\sqrt{\text{Hz}}$  Voltage Noise
- 4V/ $\mu$ s Slew Rate
- 4 $\mu$ V/°C Drift
- 130dB Channel Separation

## APPLICATIONS

- Sample-and-Hold (Drives Large Hold Capacitors)
- A/D and D/A Converters
- Photodiode Amplifiers
- Voltage-to-Frequency Converters

## DESCRIPTION

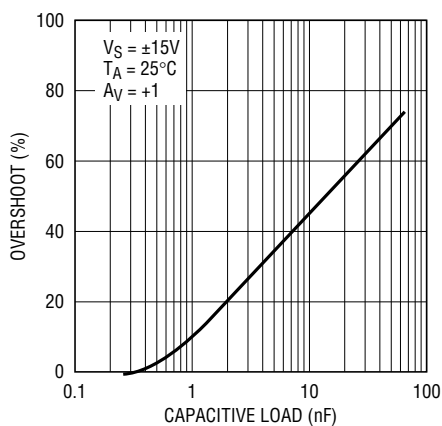
The LT1457 is a dual, JFET input op amp optimized for handling large capacitive loads in combination with precision performance.

Precision specifications include 220 $\mu$ V offset voltage in plastic and surface mount packages. At 70°C input bias current is 50pA, input offset current is 20pA. Channel separation is 130dB.

Other dual JFET input op amps from Linear Technology include the LT1057, which is three times faster than the LT1457 but at the expense of significantly lower capacitive load handling capability; and the LT1113 with 4.5nV/ $\sqrt{\text{Hz}}$  voltage noise.

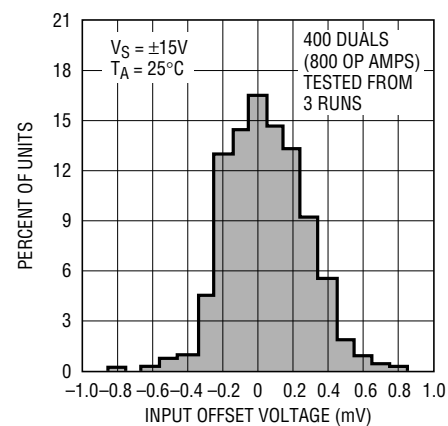
## TYPICAL PERFORMANCE CHARACTERISTICS

Capacitive Load Handling



LT1457 • TA01

Input Offset Voltage Distribution  
 S8 Package



LT1457 • TA02

### ABSOLUTE MAXIMUM RATINGS

Supply Voltage .....  $\pm 20V$   
 Differential Input Voltage .....  $\pm 40V$   
 Input Voltage ..... Equal to Supply Voltages  
 Output Short-Circuit Duration ..... Indefinite  
 Operating Temperature Range .....  $-40^{\circ}C$  to  $85^{\circ}C$   
 Storage Temperature Range .....  $-65^{\circ}C$  to  $150^{\circ}C$   
 Lead Temperature (Soldering, 10 sec) .....  $300^{\circ}C$

### PACKAGE/ORDER INFORMATION

<p>N8 PACKAGE 8-LEAD PLASTIC DIP <math>T_{JMAX} = 115^{\circ}C</math>, <math>\theta_{JA} = 130^{\circ}C/W</math></p>	ORDER PART NUMBER
	LT1457ACN8 LT1457CN8
<p>S8 PACKAGE 8-LEAD PLASTIC SOIC NOTE: THIS PIN CONFIGURATION DIFFERS FROM THE 8-LEAD DIP PIN LOCATIONS. INSTEAD, IT FOLLOWS THE INDUSTRY STANDARD LT1013DS8 SO PACKAGE CONFIGURATION. <math>T_{JMAX} = 130^{\circ}C</math>, <math>\theta_{JA} = 190^{\circ}C/W</math></p>	LT1457S8
	S8 PART MARKING
	1457

Consult factory for Industrial and Military grade parts.

### ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$ , $T_A = 25^{\circ}C$ , $V_{CM} = 0V$ unless otherwise noted. (Note 1)

SYMBOL	PARAMETER	CONDITIONS	LT1457AC			LT1457C/LT1457S8			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OS}$	Input Offset Voltage	LT1457AC/C LT1457S8		150	450		200	800	$\mu V$ $\mu V$
$I_{OS}$	Input Offset Current	Fully Warmed Up		3	40		4	50	pA
$I_B$	Input Bias Current	Fully Warmed Up		$\pm 5$	$\pm 50$		$\pm 7$	$\pm 75$	pA
	Input Resistance-Differential -Common-Mode	$V_{CM} = -11V$ to $8V$ $V_{CM} = 8V$ to $11V$		$10^{12}$			$10^{12}$		$\Omega$
				$10^{12}$			$10^{12}$		$\Omega$
				$10^{11}$			$10^{11}$		$\Omega$
	Input Capacitance			4			4		pF
$e_n$	Input Noise Voltage	0.1Hz to 10Hz		2.0			2.1		$\mu V_{p-p}$
$e_n$	Input Noise Voltage Density	$f_0 = 10Hz$		26			28		$nV/\sqrt{Hz}$
		$f_0 = 1kHz$ (Note 2)		13	22		14	24	$nV/\sqrt{Hz}$
$i_n$	Input Noise Current Density	$f_0 = 10Hz, 1kHz$ (Note 3)		1.5	4		1.8	6	$fA/\sqrt{Hz}$
$A_{VOL}$	Large-Signal Voltage Gain	$V_O = \pm 10V$ , $R_L = 2k$	150	350		100	300		V/mV
		$V_O = \pm 10V$ , $R_L = 1k$	120	250		80	220		V/mV
	Input Voltage Range		$\pm 10.5$	14.3		$\pm 10.5$	14.3		V
					-11.5			-11.5	
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.5V$	86	100		82	98		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 18V$	88	103		86	102		dB
$V_{OUT}$	Output Voltage Swing	$R_L = 2k$	$\pm 12$	$\pm 13$		$\pm 12$	$\pm 13$		V
SR	Slew Rate		2	4		2	4		V/ $\mu s$

**ELECTRICAL CHARACTERISTICS**  $V_S = \pm 15V, T_A = 25^\circ C, V_{CM} = 0V$  unless otherwise noted. (Note 1)

SYMBOL	PARAMETER	CONDITIONS	LT1457AC			LT1457C/LT1457S8			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
GBW	Gain-Bandwidth Product	(Note 5)	1.0	1.7		1.0	1.7		MHz
$I_S$	Supply Current Per Amplifier			1.8	3.0		1.8	3.0	mA
	Channel Separation	DC to 5kHz, $V_{IN} = \pm 10V$		132			130		dB

**ELECTRICAL CHARACTERISTICS**  $V_S = \pm 15V, V_{CM} = 0V, 0^\circ C \leq T_A \leq 70^\circ C$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1457AC			LT1457C/LT1457S8			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OS}$	Input Offset Voltage	LT1457AC/C LT1457S8	●	250	900		330	1500	$\mu V$
			●				400	1900	$\mu V$
	Average Temperature Coefficient of Input Offset Voltage (Note 4)		●	3	10		4	16	$\mu V/^\circ C$
$I_{OS}$	Input Offset Current	Warmed Up, $T_A = 70^\circ C$		18	150		20	250	pA
$I_B$	Input Bias Current	Warmed Up, $T_A = 70^\circ C$		$\pm 50$	$\pm 250$		$\pm 60$	$\pm 350$	pA
$A_{VOL}$	Large-Signal Voltage Gain	$V_O = \pm 10V, R_L = 2k$	●	70	220		50	200	V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.4V$	●	85	98		80	96	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 18V$	●	87	102		84	100	dB
$V_{OUT}$	Output Voltage Swing	$R_L = 2k$	●	$\pm 12$	$\pm 12.8$		$\pm 12$	$\pm 12.8$	V
$I_S$	Supply Current Per Amplifier	$T_A = 70^\circ C$	●		3.2			3.2	mA
				1.7			1.7		mA

**ELECTRICAL CHARACTERISTICS**  $V_S = \pm 15V, V_{CM} = 0V, -40^\circ C \leq T_A \leq 85^\circ C$ , unless otherwise noted. (Note 6)

SYMBOL	PARAMETER	CONDITIONS	LT1457AC			LT1457C/LT1457S8			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OS}$	Input Offset Voltage	LT1457AC/C LT1457S8	●	350	1100		400	1800	$\mu V$
			●				500	2300	$\mu V$
	Average Temperature Coefficient of Input Offset Voltage		●	3	10		4	16	$\mu V/^\circ C$
$I_{OS}$	Input Offset Current	Warmed Up, $T_A = 85^\circ C$		0.1	0.5		0.1	0.6	nA
$I_B$	Input Bias Current	Warmed Up, $T_A = 85^\circ C$		$\pm 0.2$	$\pm 0.7$		$\pm 0.2$	$\pm 0.9$	nA
$A_{VOL}$	Large-Signal Voltage Gain	$V_O = \pm 10V, R_L = 2k$	●	40	120		30	110	V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.4V$	●	84	97		80	95	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 5V$ to $\pm 17V$	●	86	100		83	98	dB
$V_{OUT}$	Output Voltage Swing	$R_L = 2k$	●	$\pm 12$	$\pm 12.7$		$\pm 12$	$\pm 12.6$	V
$I_S$	Supply Current Per Amplifier	$T_A = -40^\circ C$			3.8			3.8	mA
		$T_A = 85^\circ C$		1.7			1.7		mA

The ● denotes the specifications which apply over the full operating temperature range.

**Note 1:** Typical parameters are defined as the 60% yield of distributions of individual amplifiers; i.e., out of 100 LT1457s (200 op amps) typically 120 will be better than the indicated specification.

**Note 2:** This parameter is tested on a sample basis only.

**Note 3:** Current noise is calculated from the formula:  $i_n = (2qI_b)^{1/2}$ , where  $q = 1.6 \times 10^{-19}$  coulomb. The noise of source resistors up to 1G $\Omega$  swamps the contribution of current noise.

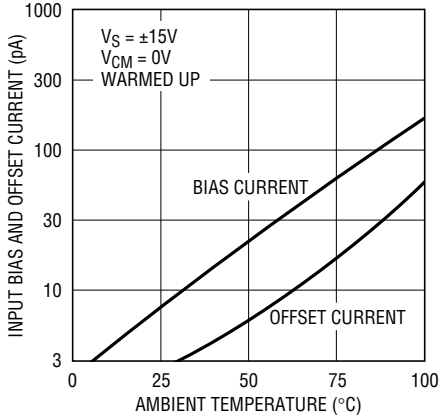
**Note 4:** This parameter is not 100% tested.

**Note 5:** Gain-Bandwidth product is not tested. It is guaranteed by design and by inference from the slew rate measurement.

**Note 6:** The LT1457 is not tested and not quality-assurance-sampled at  $-40^\circ C$  and at  $85^\circ C$ . These specifications are guaranteed by design, correlation, and/or inference from  $0^\circ C$ ,  $25^\circ C$ , and  $70^\circ C$  tests.

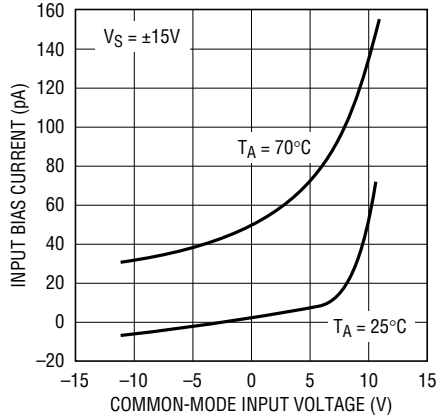
# TYPICAL PERFORMANCE CHARACTERISTICS

**Input Bias and Offset Current vs Temperature**



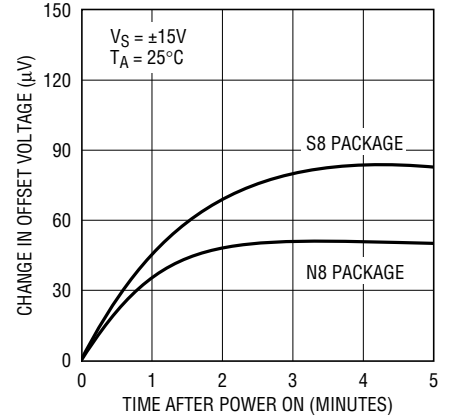
LT1457 • TPC01

**Input Bias Current Over the Common-Mode Range**



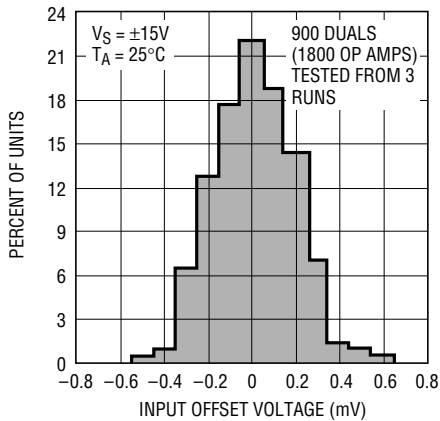
LT1457 • TPC02

**Warm-Up Drift**



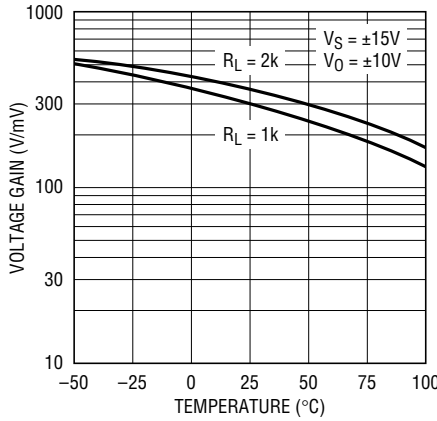
LT1457 • TPC03

**Input Offset Voltage Distribution N8 Package**



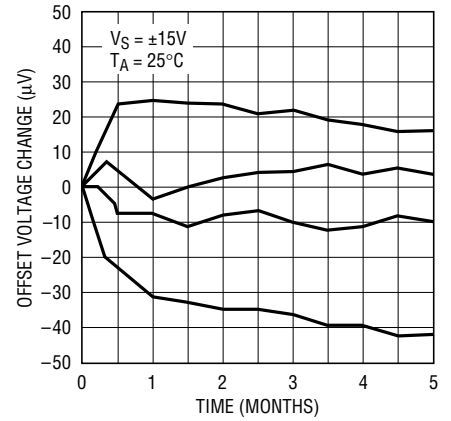
LT1457 • TPC04

**Voltage Gain vs Temperature**



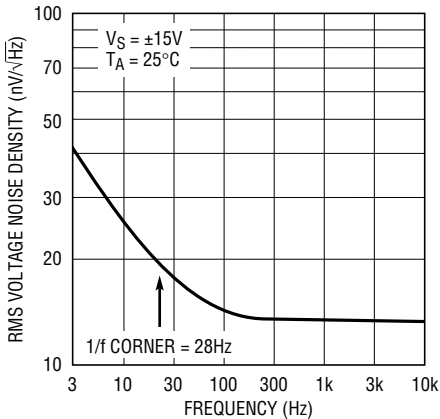
LT1457 • TPC05

**Long Term Drift of Representative Units**



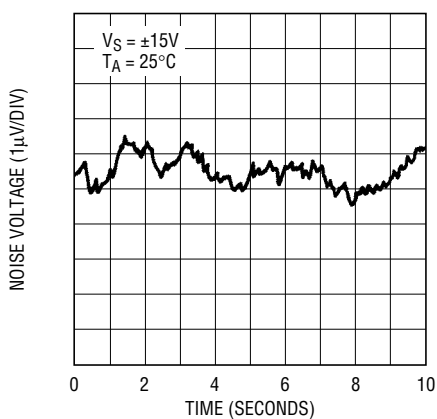
LT1457 • TPC06

**Voltage Noise vs Frequency**



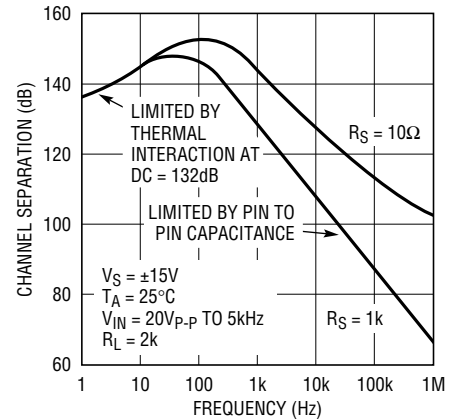
LT1457 • TPC07

**0.1Hz to 10Hz Noise**



LT1457 • TPC08

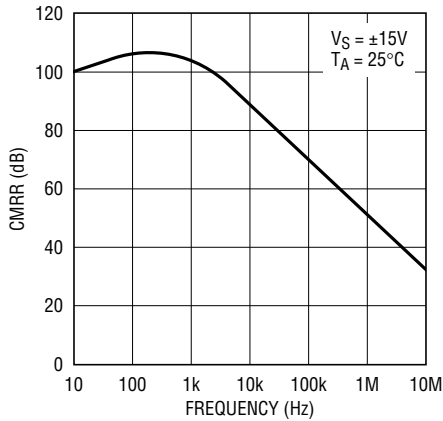
**Channel Separation vs Frequency**



LT1457 • TPC09

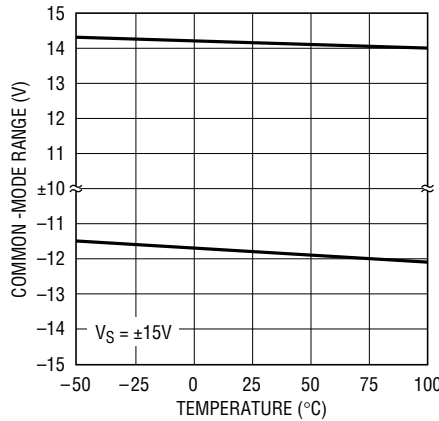
# TYPICAL PERFORMANCE CHARACTERISTICS

**Common-Mode Rejection Ratio vs Frequency**



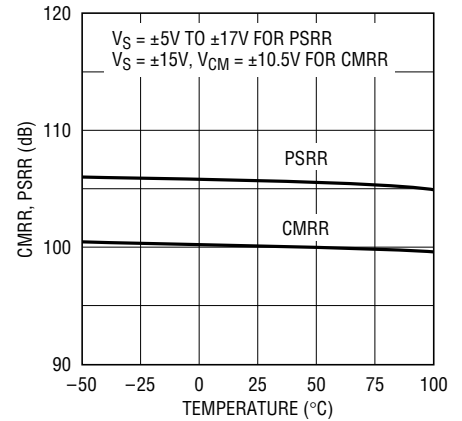
LT1457 • TPC10

**Common-Mode Range vs Temperature**



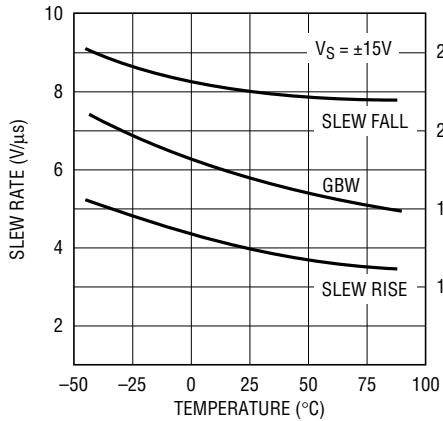
LT1457 • TPC11

**Common-Mode and Power Supply Rejections vs Temperature**



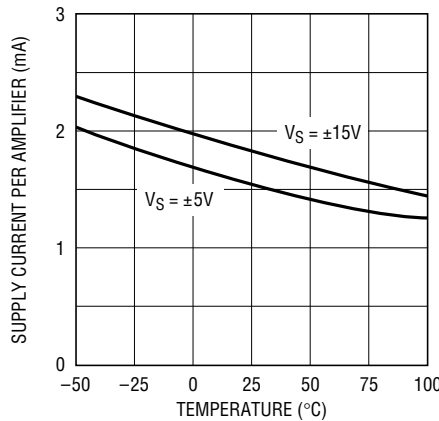
LT1457 • TPC12

**Slew Rate, Gain-Bandwidth Product vs Temperature**



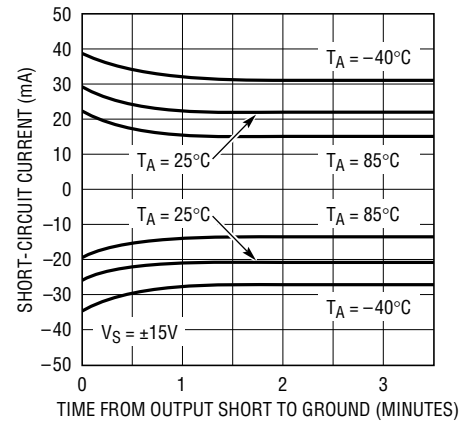
LT1457 • TPC13

**Supply Current vs Temperature**



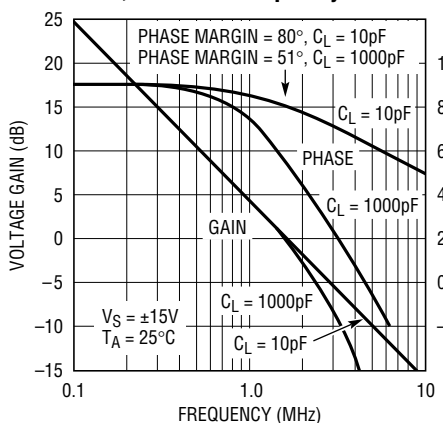
LT1457 • TPC14

**Short-Circuit Current vs Time (One Output Shorted to Ground)**



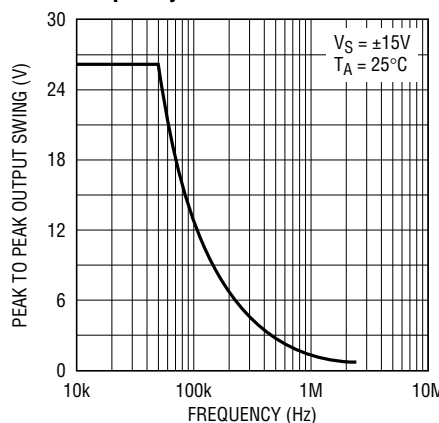
LT1457 • TPC15

**Gain, Phase vs Frequency**



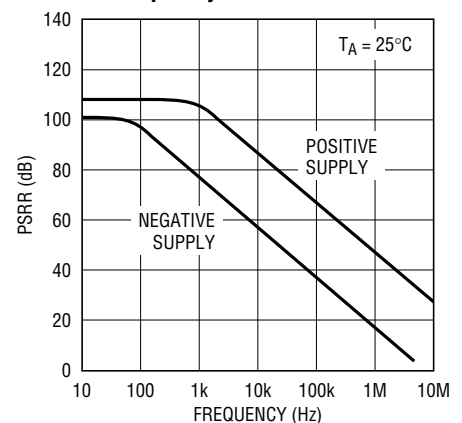
LT1457 • TPC16

**Undistorted Output Swing vs Frequency**



LT1457 • TPC17

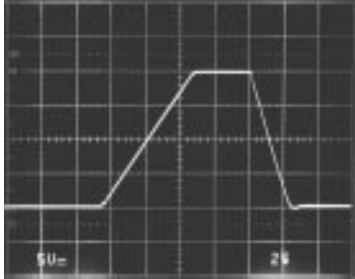
**Power Supply Rejection Ratio vs Frequency**



LT1457 • TPC18

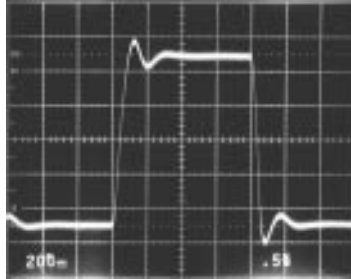
## TYPICAL PERFORMANCE CHARACTERISTICS

Large-Signal Response  
 $A_V = 1$ ,  $C_L = 100\text{pF}$



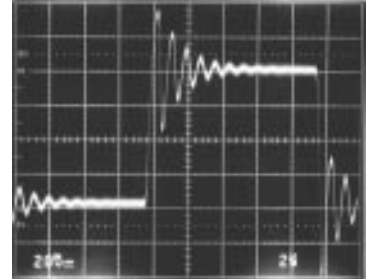
LT1457 TPC19

Small-Signal Response  
 $A_V = 1$ ,  $C_L = 1000\text{pF}$



LT1457 TPC20

Small-Signal Response  
 $A_V = 1$ ,  $C_L = 10,000\text{pF}$



LT1457 TPC21

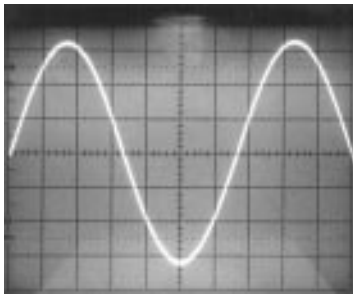
## APPLICATIONS INFORMATION

### Phase Reversal Protection

Most industry standard JFET input single, dual, and quad op amps (e.g., LF156, LF351, LF353, LF411, LF412, OP-15, OP-16, OP-215, and TL084) exhibit phase reversal at the output when the negative common-mode limit at the input is exceeded (i.e., below  $-12\text{V}$  with  $\pm 15\text{V}$  supplies). The photos show a  $\pm 16\text{V}$  sine wave input (A), the response

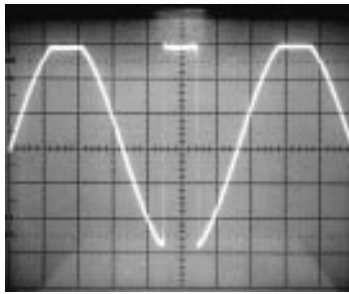
of an LF412A in the unity gain follower mode (B), and the response of the LT1457 (C).

The phase reversal of photo (B) can cause lock-up in servo systems. The LT1457 does not phase-reverse due to a unique phase reversal protection circuit.



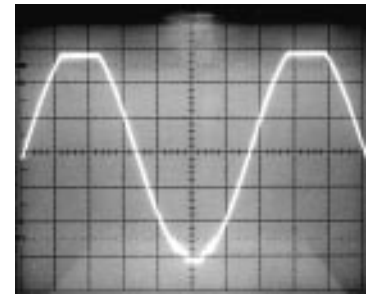
LT1457 AI01

(A)  $\pm 16\text{V}$  Sine Wave Input



LT1457 AI02

(B) LF412A Output



LT1457 AI03

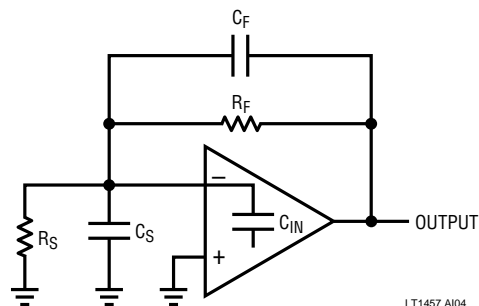
(C) LT1457 Output

All Photos 5V/Div Vertical Scale, 50 $\mu\text{s}$ /Div Horizontal Scale

## APPLICATIONS INFORMATION

### High Speed Operation

When the feedback around the op amp is resistive ( $R_F$ ), a pole will be created with  $R_F$ , the source resistance and capacitance ( $R_S, C_S$ ), and the amplifier input capacitance ( $C_{IN} \approx 4\text{pF}$ ). In low closed loop gain configurations and with  $R_S$  and  $R_F$  in the kilohm range, this pole can create excess phase shift and even oscillation on high speed amplifiers. Because the LT1457's phase margin is very high, this problem is minimal. However, a small capacitor ( $C_F$ ) in parallel with  $R_F$  eliminates this problem. With  $R_S(C_S + C_{IN}) = R_F C_F$ , the effect of the feedback pole is completely removed.

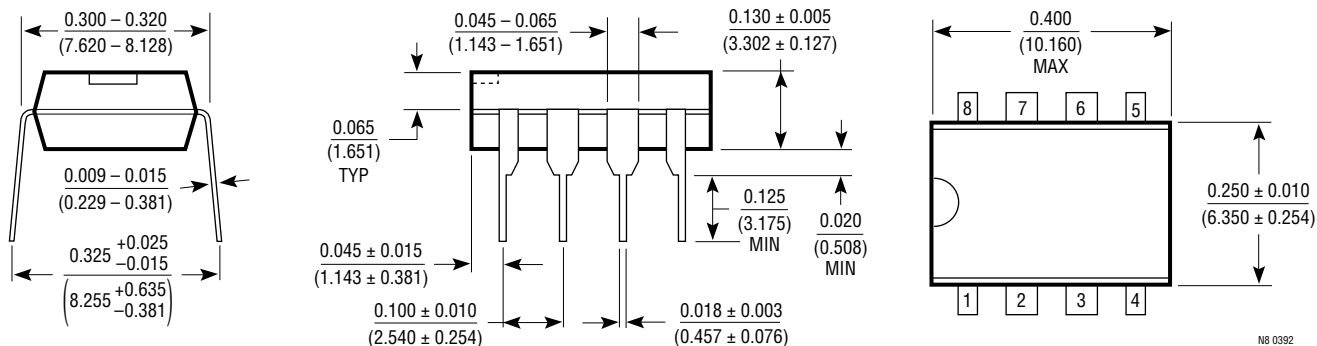


LT1457 A104

## PACKAGE DESCRIPTION

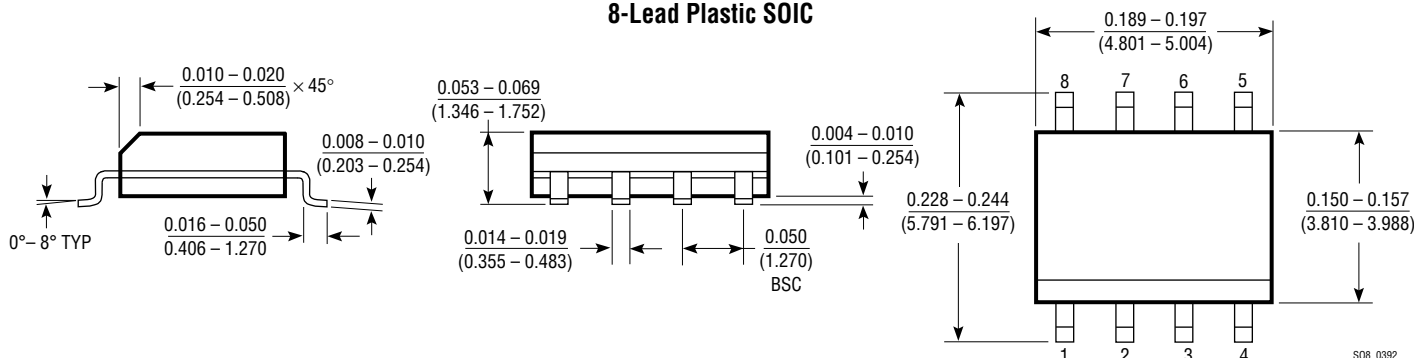
Dimension in inches (millimeters) unless otherwise noted.

### N8 Package 8-Lead Plastic DIP



N8 0392

### S8 Package 8-Lead Plastic SOIC



S08 0392

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