SN74AVC1T45 Single-Bit Dual-Supply Bus Transceiver with Configurable Voltage Translation and 3-State Outputs

1 Features

- Available in the Texas Instruments NanoFree™ Package
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.2-V to 3.6-V Power-Supply Range
- V_{CC} Isolation Feature - If Either V_{CC} Input Is At GND, Both Ports Are In The High-Impedance State
- DIR Input Circuit Referenced to V_{CCA}
- ±12-mA Output Drive at 3.3 V
- I/Os Are 4.6-V Tolerant
- I_{off} Supports Partial-Power-Down Mode Operation
- Typical Max Data Rates
  - 500 Mbps (1.8-V to 3.3-V Translation)
  - 320 Mbps (<1.8-V to 3.3-V Translation)
  - 320 Mbps (Translate to 2.5 V or 1.8 V)
  - 280 Mbps (Translate to 1.5 V)
  - 240 Mbps (Translate to 1.2 V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - ±2000-V Human Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - ±1000-V Charged-Device Model (C101)

2 Applications

- Personal Electronic
- Industrial
- Enterprise
- Telecom

3 Description

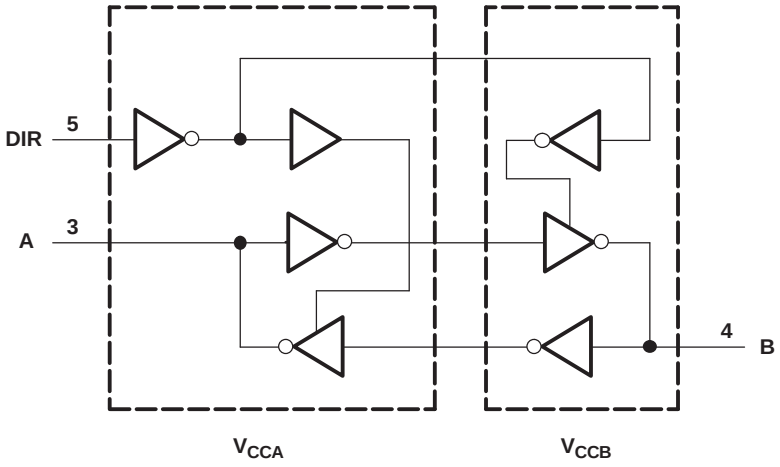
This single-bit noninverting bus transceiver uses two separate configurable power-supply rails. The SN74AVC1T45 is optimized to operate with V_{CCA}/V_{CCB} set at 1.4 V to 3.6 V. It is operational with V_{CCA}/V_{CCB} as low as 1.2 V. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.2 V to 3.6 V. This allows for universal low-voltage, bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AVC1T45	SOT (6)	2.90 mm × 1.60 mm
		2.00 mm × 1.25 mm
		1.60 mm × 1.20 mm
	DSBGA (6)	1.39 mm × 0.89 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Logic Diagram (Positive Logic)



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4 Revision History

Changes from Revision G (January 2008) to Revision H **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

5 Description (continued)

The SN74AVC1T45 is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input activate either the B-port outputs or the A-port outputs. The device transmits data from the A bus to the B bus when the B-port outputs are activated and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports always is active and must have a logic HIGH or LOW level applied to prevent excess I_{CC} and I_{CCZ}.

The SN74AVC1T45 is designed so that the DIR input is powered by V_{CCA}.

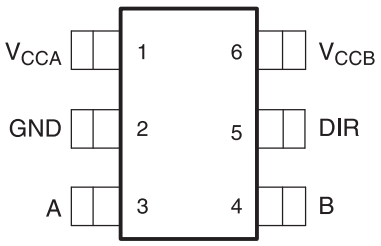
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, then both ports are in the high-impedance state.

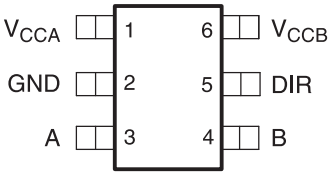
NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

6 Pin Configuration and Functions

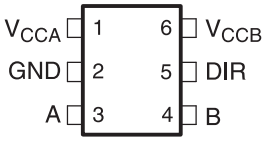
DBV PACKAGE
(TOP VIEW)



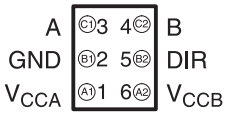
DCK PACKAGE
(TOP VIEW)



DRL PACKAGE
(TOP VIEW)



YZP PACKAGE
(BOTTOM VIEW)



See mechanical drawings in *Mechanical, Packaging, and Orderable Information* for dimensions.

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
V_{CCA}	1	P	A-port supply voltage. 1.2 V ≤ V_{CCA} ≤ 3.6 V
GND	2	G	Ground
A	3	I/O	Input/output A. Referenced to V_{CCA}.
B	4	I/O	Input/output B. Referenced to V_{CCB}.
DIR	5	I	Direction control signal
V_{CCB}	6	P	B-port supply voltage. 1.2 V ≤ V_{CCB} ≤ 3.6 V.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CCA}, V_{CCB}	Supply voltage		–0.5	4.6	V
V_I	Input voltage (2)	I/O ports (A port)	–0.5	4.6	V
		I/O ports (B port)	–0.5	4.6	
		Control inputs	–0.5	4.6	
V_O	Voltage applied to any output in the high-impedance or power-off state(2)	A port	–0.5	4.6	V
		B port	–0.5	4.6	
V_O	Voltage applied to any output in the high or low state(2) (3)	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current		–50	50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND		–100	100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current ratings are observed.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
	Machine model, per A115-A	200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.2	3.6	V
V_{CCB}	Supply voltage				1.2	3.6	V
V_{IH}	High-level input voltage	Data inputs	1.2 V to 1.95 V		V_{CCI} × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	Data inputs	1.2 V to 1.95 V			V_{CCI} × 0.35	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_{IH}	High-level input voltage	DIR (referenced to V_{CCA})	1.2 V to 1.95 V		V_{CCA} × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	DIR (referenced to V_{CCA})	1.2 V to 1.95 V			V_{CCA} × 0.35	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_I	Input voltage				0	3.6	V
V_O	Output voltage	Active state			0	V_{CCO}	V
		3-state			0	3.6	
I_{OH}	High-level output current			1.2 V		–3	mA
				1.4 V to 1.6 V		–6	
				1.65 V to 1.95 V		–8	
				2.3 V to 2.7 V		–9	
				3 V to 3.6 V		–12	
I_{OL}	Low-level output current			1.2 V		3	mA
				1.4 V to 1.6 V		6	
				1.65 V to 1.95 V		8	
				2.3 V to 2.7 V		9	
				3 V to 3.6 V		12	
Δt/Δv	Input transition rise or fall rate					5	ns/V
T_A	Operating free-air temperature				–40	85	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

7.4 Thermal Information

THERMAL METRIC(1)		SN74AVC1T45				UNIT
		DBV	DCK	DRL	YZP	
		6 PINS				
$R_{\theta JA}$	Junction-to-ambient thermal resistance	24.3	290.7	236.2	130	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	174.7	97.0	97.6	54	
$R_{\theta JB}$	Junction-to-board thermal resistance	92.4	99.2	71.0	51	
ψ_{JT}	Junction-to-top characterization parameter	61.1	2.1	8.3	1	
ψ_{JB}	Junction-to-board characterization parameter	92.0	98.4	70.8	50	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics(1) (2)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	T_A = 25°C			–40°C to 85°C		UNIT
						MIN	TYP	MAX	MIN	MAX	
V_{OH}		I_{OH} = –100 µA	$V_I = V_{IH}$	1.2 V to 3.6 V	1.2 V to 3.6 V				V_{CCO} – 0.2		V
		I_{OH} = –3 mA		1.2 V	1.2 V		0.95				
		I_{OH} = –6 mA		1.4 V	1.4 V				1.05		
		I_{OH} = –8 mA		1.65 V	1.65 V				1.2		
		I_{OH} = –9 mA		2.3 V	2.3 V				1.75		
		I_{OH} = –12 mA		3 V	3 V				2.3		
V_{OL}		I_{OL} = 100 µA	$V_I = V_{IL}$	1.2 V to 3.6 V	1.2 V to 3.6 V					0.2	V
		I_{OL} = 3 mA		1.2 V	1.2 V		0.15				
		I_{OL} = 6 mA		1.4 V	1.4 V					0.35	
		I_{OL} = 8 mA		1.65 V	1.65 V					0.45	
		I_{OL} = 9 mA		2.3 V	2.3 V					0.55	
		I_{OL} = 12 mA		3 V	3 V					0.7	
I_I	DIR	$V_I = V_{CCA}$ or GND		1.2 V to 3.6 V	1.2 V to 3.6 V	–0.25	±0.025	0.25	–1	1	µA
I_{off}	A port	V_I or V_O = 0 to 3.6 V		0 V	0 to 3.6 V	–1	±0.1	1	–5	5	µA
	B port			0 to 3.6 V	0 V	–1	±0.1	1	–5	5	
I_{OZ}	B port	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND		0 V	3.6 V	–2.5	±0.5	2.5	–5	5	µA
	A port			3.6 V	0 V	–2.5	±0.5	2.5	–5	5	
I_{CCA}		$V_I = V_{CCI}$ or GND, I_O = 0		1.2 V to 3.6 V	1.2 V to 3.6 V					10	µA
				0 V	3.6 V					–2	
				3.6 V	0 V					10	
I_{CCB}		$V_I = V_{CCI}$ or GND, I_O = 0		1.2 V to 3.6 V	1.2 V to 3.6 V					10	µA
				0 V	3.6 V					10	
				3.6 V	0 V					–2	
$I_{CCA} + I_{CCB}$ (see Table 4)		$V_I = V_{CCI}$ or GND, I_O = 0		1.2 V to 3.6 V	1.2 V to 3.6 V					20	µA
C_i	Control inputs	V_I = 3.3 V or GND		3.3 V	3.3 V		2.5				pF
C_{io}	A or B port	V_O = 3.3 V or GND		3.3 V	3.3 V		6				pF

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) V_{CCI} is the V_{CC} associated with the input port.

7.6 Switching Characteristics: V_{CCA} = 1.2 V

over recommended operating free-air temperature range, V_{CCA} = 1.2 V (see Figure 11)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V	V_{CCB} = 1.8 V	V_{CCB} = 2.5 V	V_{CCB} = 3.3 V	UNIT
			TYP	TYP	TYP	TYP	TYP	
t_{PLH}	A	B	3.3	2.7	2.4	2.3	2.4	ns
t_{PHL}			3.3	2.7	2.4	2.3	2.4	
t_{PLH}	B	A	3.3	3.1	2.9	2.8	2.7	ns
t_{PHL}			3.3	3.1	2.9	2.8	2.7	
t_{PHZ}	DIR	A	5.1	5.2	5.3	5.2	3.7	ns
t_{PLZ}			5.1	5.2	5.3	5.2	3.7	
t_{PHZ}	DIR	B	5.3	4.3	4	3.3	3.7	ns
t_{PLZ}			5.3	4.3	4	3.3	3.7	
t_{PZH} (1)	DIR	A	8.6	7.3	6.8	6.1	6.4	ns
t_{PZL} (1)			8.6	7.3	6.8	6.1	6.4	
t_{PZH} (1)	DIR	B	8.3	7.8	7.7	7.5	5.8	ns
t_{PZL} (1)			8.3	7.8	7.7	7.5	5.8	

(1) The enable time is a calculated value, derived using the formula shown in the *Enable Times* section.

7.7 Switching Characteristics: V_{CCA} = 1.5 V ± 0.1 V

over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (see Figure 11)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.9	0.7	5.6	0.6	5.2	0.5	4.2	0.5	3.8	ns
t_{PHL}			2.9	0.7	5.6	0.6	5.2	0.5	4.2	0.5	3.8	
t_{PLH}	B	A	2.6	0.6	5.5	0.4	5.3	0.3	4.9	0.3	4.8	ns
t_{PHL}			2.6	0.6	5.5	0.4	5.3	0.3	4.9	0.3	4.8	
t_{PHZ}	DIR	A	3.8	1.6	6.7	1.5	6.8	0.3	6.9	0.9	6.9	ns
t_{PLZ}			3.8	1.6	6.7	1.5	6.8	0.3	6.9	0.9	6.9	
t_{PHZ}	DIR	B	5.1	1.8	8.1	1.6	7.1	1.1	4.7	1.4	4.5	ns
t_{PLZ}			5.1	1.8	8.1	1.6	7.1	1.1	4.7	1.4	4.5	
t_{PZH} (1)	DIR	A	7.7		13.6		12.4		9.6		9.3	ns
t_{PZL} (1)			7.7		13.6		12.4		9.6		9.3	
t_{PZH} (1)	DIR	B	6.7		12.3		12		11.1		10.7	ns
t_{PZL} (1)			6.7		12.3		12		11.1		10.7	

(1) The enable time is a calculated value, derived using the formula shown in the *Enable Times* section.

7.8 Switching Characteristics: V_{CCA} = 1.8 V ± 0.15 V

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (see Figure 11)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.7	0.6	5.3	0.5	5	0.4	3.9	0.4	3.4	ns
t_{PHL}			2.7	0.6	5.3	0.5	5	0.4	3.9	0.4	3.4	
t_{PLH}	B	A	2.3	0.5	5.2	0.4	5	0.3	4.6	0.2	4.4	ns
t_{PHL}			2.3	0.5	5.2	0.4	5	0.3	4.6	0.2	4.4	
t_{PHZ}	DIR	A	3.8	1.6	5.9	1.6	5.9	1.6	5.9	0.5	6	ns
t_{PLZ}			3.8	1.6	5.9	1.6	5.9	1.6	5.9	0.5	6	
t_{PHZ}	DIR	B	5	1.8	7.7	1.4	6.8	1	4.4	1.4	5.3	ns
t_{PLZ}			5	1.8	7.7	1.4	6.8	1	4.4	1.4	5.3	
t_{PZH} (1)	DIR	A	7.3		12.9		11.8		9		8.7	ns
t_{PZL} (1)			7.3		12.9		11.8		9		8.7	
t_{PZH} (1)	DIR	B	6.5		11.2		10.9		9.8		9.4	ns
t_{PZL} (1)			6.5		11.2		10.9		9.8		9.4	

(1) The enable time is a calculated value, derived using the formula shown in the *Enable Times* section.

7.9 Switching Characteristics: V_{CCA} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (see Figure 11)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.6	0.5	4.9	0.4	4.6	0.3	3.4	0.3	3	ns
t_{PHL}			2.6	0.5	4.9	0.4	4.6	0.3	3.4	0.3	3	
t_{PLH}	B	A	2.2	0.4	4.2	0.3	3.8	0.2	3.4	0.2	3.3	ns
t_{PHL}			2.2	0.4	4.2	0.3	3.8	0.2	3.4	0.2	3.3	
t_{PHZ}	DIR	A	2.8	0.3	3.8	0.8	3.8	0.4	3.8	0.5	3.8	ns
t_{PLZ}			2.8	0.3	3.8	0.8	3.8	0.4	3.8	0.5	3.8	
t_{PHZ}	DIR	B	4.9	2	7.6	1.5	6.5	0.6	4.1	1	4	ns
t_{PLZ}			4.9	2	7.6	1.5	6.5	0.6	4.1	1	4	
t_{PZH} (1)	DIR	A	7.1		11.8		10.3		7.5		7.3	ns
t_{PZL} (1)			7.1		11.8		10.3		7.5		7.3	
t_{PZH} (1)	DIR	B	5.4		8.6		8.1		7		6.6	ns
t_{PZL} (1)			5.4		8.6		8.1		7		6.6	

(1) The enable time is a calculated value, derived using the formula shown in the *Enable Times* section.

7.10 Switching Characteristics: V_{CCA} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (see Figure 11)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.6	0.4	4.7	0.3	4.4	0.2	3.3	0.2	2.8	ns
t_{PHL}			2.6	0.4	4.7	0.3	4.4	0.2	3.3	0.2	2.8	
t_{PLH}	B	A	2.2	0.4	3.8	0.3	3.4	0.2	3	0.1	2.8	ns
t_{PHL}			2.2	0.4	3.8	0.3	3.4	0.2	3	0.1	2.8	
t_{PHZ}	DIR	A	3.1	1.3	4.3	1.3	4.3	1.3	4.3	1.3	4.3	ns
t_{PLZ}			3.1	1.3	4.3	1.3	4.3	1.3	4.3	1.3	4.3	
t_{PHZ}	DIR	B	4	0.7	7.4	0.6	6.5	0.7	4	1.5	4.9	ns
t_{PLZ}			4	0.7	7.4	0.6	6.5	0.7	4	1.5	4.9	
t_{PZH} (1)	DIR	A	6.2		11.2		9.9		7		6.7	ns
t_{PZL} (1)			6.2		11.2		9.9		7		6.7	
t_{PZH} (1)	DIR	B	5.7		8.9		8.5		7.2		6.8	ns
t_{PZL} (1)			5.7		8.9		8.5		7.2		6.8	

(1) The enable time is a calculated value, derived using the formula shown in the *Enable Times* section.

7.11 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CCA} = V_{CCB} = 1.2 V	V_{CCA} = V_{CCB} = 1.5 V	V_{CCA} = V_{CCB} = 1.8 V	V_{CCA} = V_{CCB} = 2.5 V	V_{CCA} = V_{CCB} = 3.3 V	UNIT
			TYP	TYP	TYP	TYP	TYP	
C_{pdA} (1)	A-port input, B-port output	C_L = 0 pF, f = 10 MHz, $t_r = t_f$ = 1 ns	3	3	3	3	4	pF
	B-port input, A-port output		13	13	14	15	15	
C_{pdB} (1)	A-port input, B-port output	C_L = 0 pF, f = 10 MHz, $t_r = t_f$ = 1 ns	13	13	14	15	15	pF
	B-port input, A-port output		3	3	3	3	3	

(1) Power dissipation capacitance per transceiver

7.12 Typical Characteristics

7.12.1 Typical Propagation Delay (A to B) vs Load Capacitance

T_A = 25°C, V_{CCA} = 1.2 V

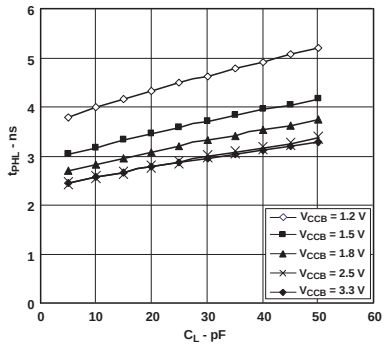


Figure 1. Typical Propagation Delay of High-to-Low (A to B) vs Load Capacitance T_A = 25°C, V_{CCA} = 1.2 V

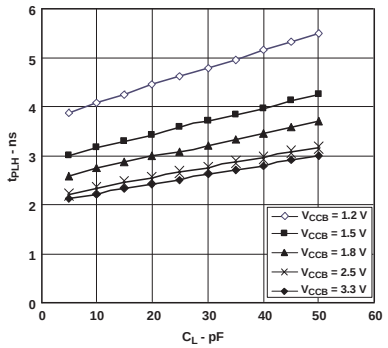


Figure 2. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance T_A = 25°C, V_{CCA} = 1.2 V

7.12.2 Typical Propagation Delay (A to B) vs Load Capacitance

T_A = 25°C, V_{CCA} = 1.5 V

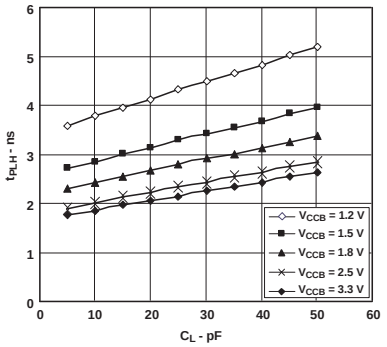


Figure 3. Typical Propagation Delay of High-to-Low (A to B) vs Load Capacitance T_A = 25°C, V_{CCA} = 1.5 V

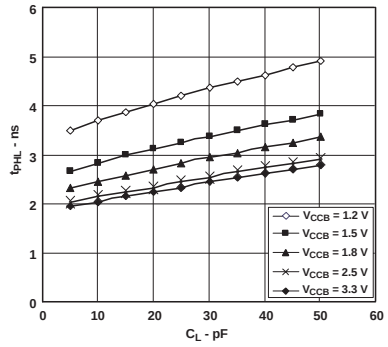


Figure 4. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance T_A = 25°C, V_{CCA} = 1.5 V

7.12.3 Typical Propagation Delay (A to B) vs Load Capacitance

T_A = 25°C, V_{CCA} = 1.8 V

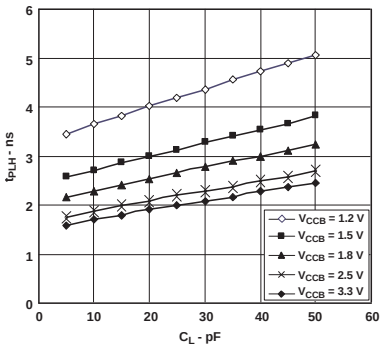


Figure 5. Typical Propagation Delay of High-to-Low (A to B) vs Load Capacitance T_A = 25°C, V_{CCA} = 1.8 V

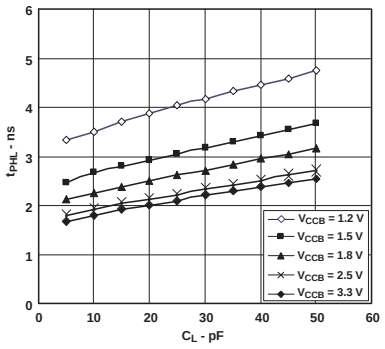


Figure 6. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance T_A = 25°C, V_{CCA} = 1.8 V

7.12.4 Typical Propagation Delay (A to B) vs Load Capacitance

T_A = 25°C, V_{CCA} = 2.5 V

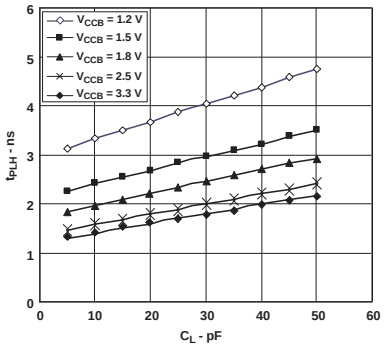


Figure 7. Typical Propagation Delay of High-to-Low (A to B) vs Load Capacitance T_A = 25°C, V_{CCA} = 2.5 V

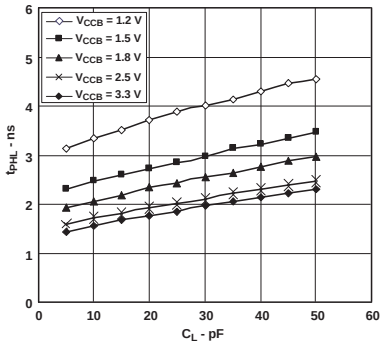


Figure 8. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance T_A = 25°C, V_{CCA} = 2.5 V

7.12.5 Typical Propagation Delay (A to B) vs Load Capacitance

T_A = 25°C, V_{CCA} = 3.3 V

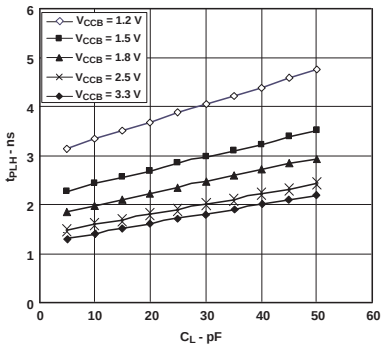


Figure 9. Typical Propagation Delay of High-to-Low (A to B) vs Load Capacitance T_A = 25°C, V_{CCA} = 3.3 V

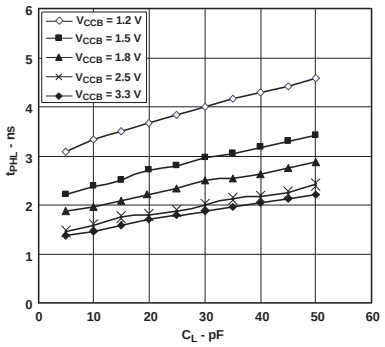
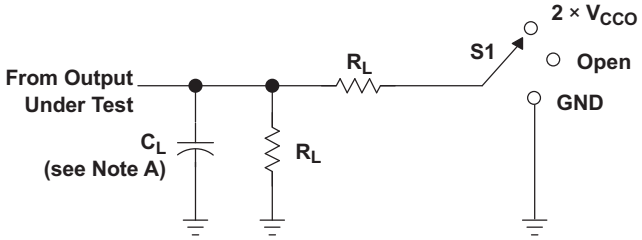


Figure 10. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance T_A = 25°C, V_{CCA} = 3.3 V

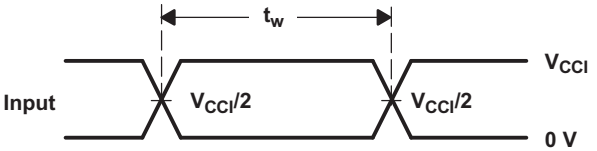
8 Parameter Measurement Information



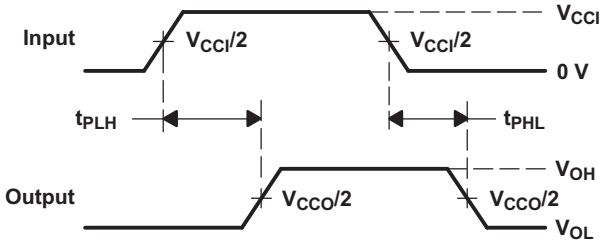
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CCO}
t_{PHZ}/t_{PZH}	GND

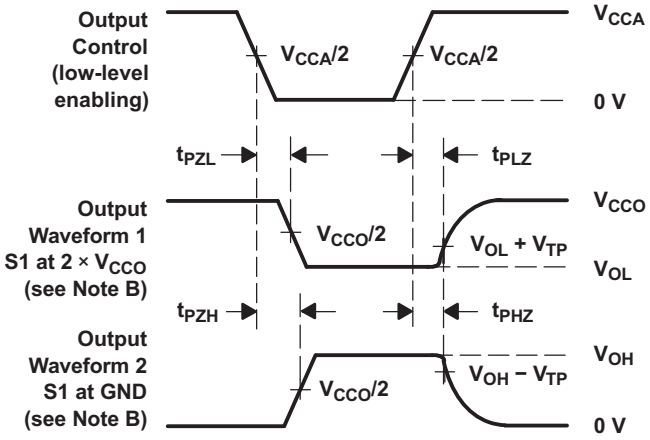
V_{CCO}	C_L	R_L	V_{TP}
1.2 V	15 pF	2 kW	0.1 V
1.5 V ± 0.1 V	15 pF	2 kW	0.1 V
1.8 V ± 0.15 V	15 pF	2 kW	0.15 V
2.5 V ± 0.2 V	15 pF	2 kW	0.15 V
3.3 V ± 0.3 V	15 pF	2 kW	0.3 V



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz, Z_O = 50 W, dv/dt ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. V_{CCI} is the V_{CC} associated with the input port.
I. V_{CCO} is the V_{CC} associated with the output port.

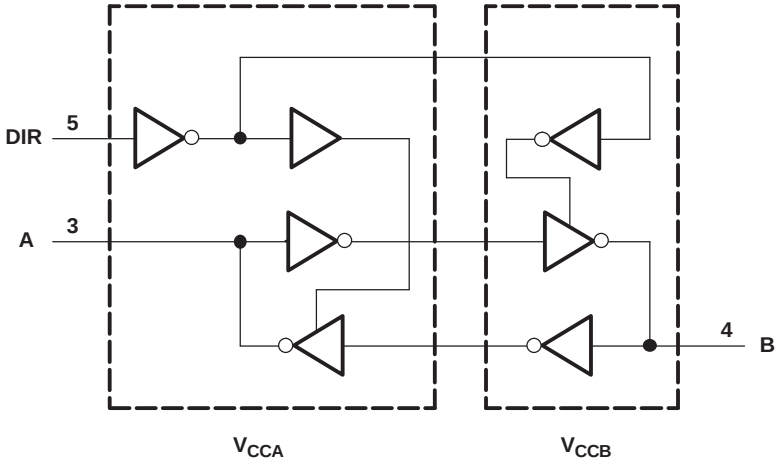
Figure 11. Load Circuit and Voltage Waveforms

9 Detailed Description

9.1 Overview

The SN74AVC1T45 is single-bit, dual-supply, noninverting voltage level translation. Pin A and direction control pin are support by V_{CCA} and pin B is support by V_{CCB}. The A port is able to accept I/O voltages ranging from 1.2 V to 3.6 V, while the B port can accept I/O voltages from 1.2 to 3.6 V. The high on DIR allows data transmission from A to B and a low on DIR allows data transmission from B to A.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.2-V to 3.6-V Power-Supply Range

Both V_{CCA} and V_{CCB} can be supplied at any voltage between 1.2 V and 3.6 V making the device suitable for translating between any of the voltage nodes (1.2-V, 1.8-V, 2.5-V and 3.3-V).

9.3.2 Support High-Speed Translation

SN74AVC1T45 can support high data-rate application. The translated signal data rate can be up to 500 Mbps when signal is translated from 1.8 V to 3.3 V.

9.3.3 I_{off} Supports Partial-Power-Down Mode Operation

I_{off} will prevent backflow current by disabling I/O output circuits when device is in partial-power-down mode.

9.4 Device Functional Modes

Table 1. Function Table(1)

INPUT DIR	OPERATION
L	B data to A bus
H	A data to B bus

(1) Input circuits of the data I/Os always are active.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN74AVC1T45 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The maximum data rate can be up to 500 Mbps when device translate signal from 1.8 V to 3.3 V.

10.1.1 Enable Times

Calculate the enable times for the SN74AVC1T45 using the following formulas:

- t_{PZH} (DIR to A) = t_{PLZ} (DIR to B) + t_{PLH} (B to A)
- t_{PZL} (DIR to A) = t_{PHZ} (DIR to B) + t_{PHL} (B to A)
- t_{PZH} (DIR to B) = t_{PLZ} (DIR to A) + t_{PLH} (A to B)
- t_{PZL} (DIR to B) = t_{PHZ} (DIR to A) + t_{PHL} (A to B)

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the SN74AVC1T45 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

10.2 Typical Applications

10.2.1 Unidirectional Logic Level-Shifting Application

Figure 12 shows an example of the SN74AVC1T45 being used in a unidirectional logic level-shifting application.

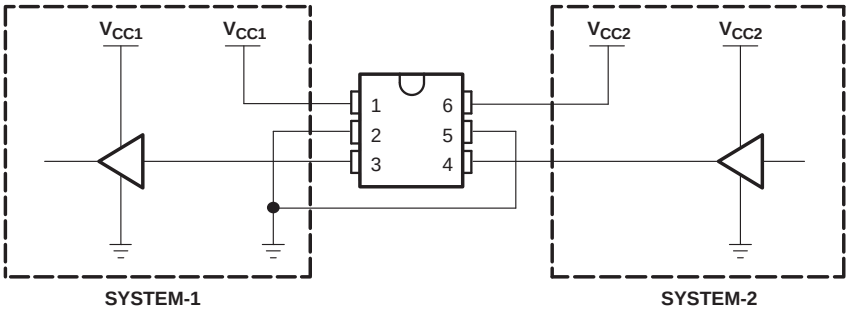


Figure 12. Unidirectional Logic Level-Shifting Application

PIN	NAME	FUNCTION	DESCRIPTION
1	V_{CCA}	V_{CC1}	SYSTEM-1 supply voltage (1.2 V to 3.6 V)
2	GND	GND	Device GND
3	A	OUT	Output level depends on V_{CC1} voltage.
4	B	IN	Input threshold value depends on V_{CC2} voltage.
5	DIR	DIR	GND (low level) determines B-port to A-port direction.
6	V_{CCB}	V_{CC2}	SYSTEM-2 supply voltage (1.2 V to 3.6 V)

10.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 2.

Table 2. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input voltage range	1.2 V to 3.6 V
Output voltage range	1.2 V to 3.6 V

10.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AVC1T45 device to determine the input voltage range. For a valid logic-high, the value must exceed the VIH of the input port. For a valid logic low the value must be less than the VIL of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74AVC1T45 device is driving to determine the output voltage range.

10.2.1.3 Application Curve

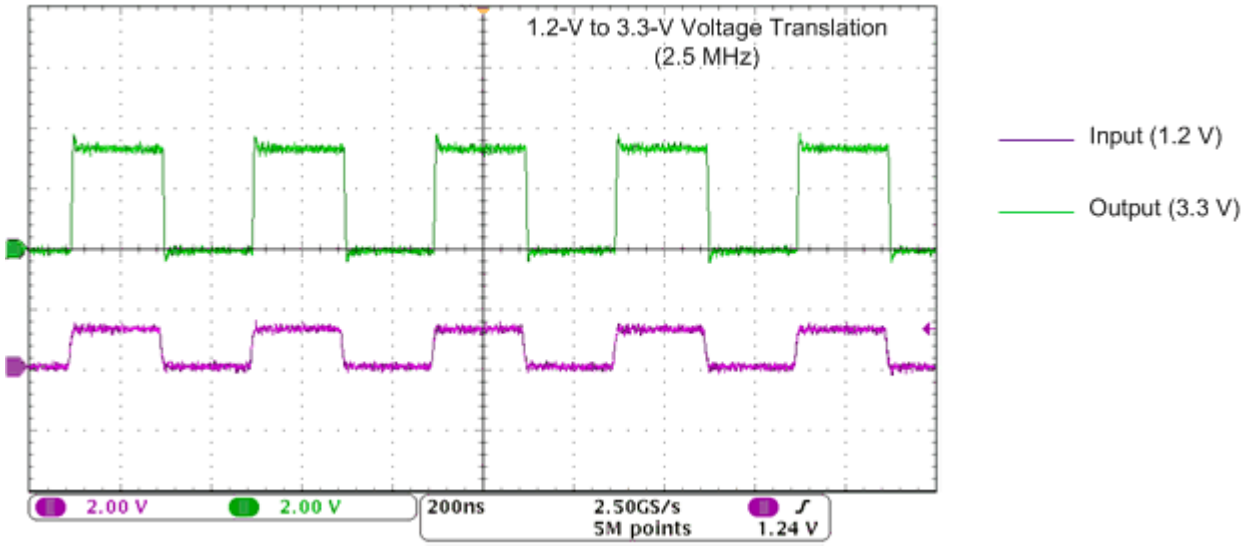


Figure 13. Translation Up (1.2 V to 3.3 V) at 2.5 MHz

10.2.2 Bidirectional Logic Level-Shifting Application

Figure 14 shows the SN74AVC1T45 being used in a bidirectional logic level-shifting application. Because the SN74AVC1T45 does not have an output-enable (OE) pin, the system designer should take precautions to avoid bus contention between SYSTEM-1 and SYSTEM-2 when changing directions.

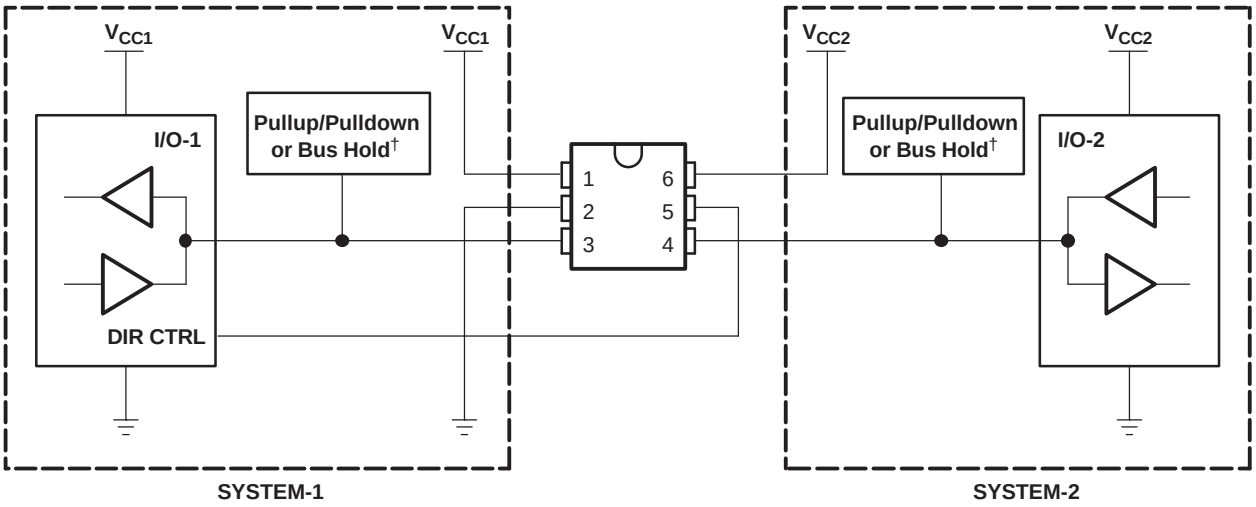


Figure 14. Bidirectional Logic Level-Shifting Application

The following table shows data transmission from SYSTEM-1 to SYSTEM-2 and then from SYSTEM-2 to SYSTEM-1.

Table 3. Data Transmission: SYSTEM-1 and SYSTEM-2

STATE	DIR CTRL	I/O-1	I/O-2	DESCRIPTION
1	H	Out	In	SYSTEM-1 data to SYSTEM-2
2	H	Hi-Z	Hi-Z	SYSTEM-2 is getting ready to send data to SYSTEM-1. I/O-1 and I/O-2 are disabled. The bus-line state depends on pullup or pulldown.(1)
3	L	Hi-Z	Hi-Z	DIR bit is flipped. I/O-1 and I/O-2 still are disabled. The bus-line state depends on pullup or pulldown.(1)
4	L	In	Out	SYSTEM-2 data to SYSTEM-1

(1) SYSTEM-1 and SYSTEM-2 must use the same conditions, i.e., both pullup or both pulldown.

10.2.2.1 Design Requirements

Refer to *Design Requirements*.

10.2.2.2 Detailed Design Procedure

Refer to *Detailed Design Procedure*.

10.2.2.3 Application Curve

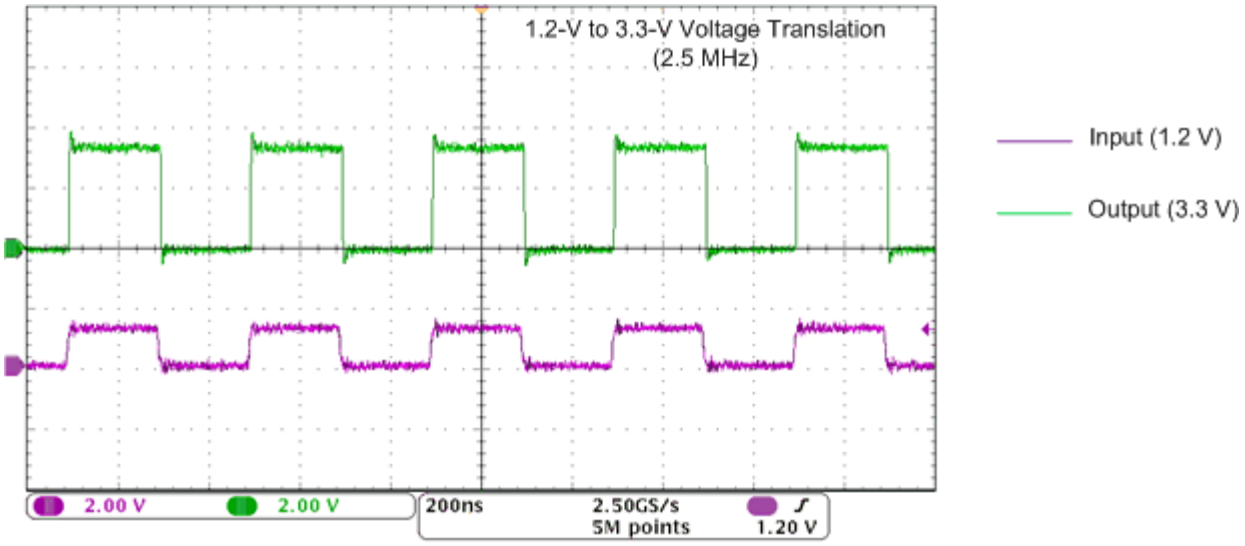


Figure 15. Translation Up (1.2 V to 3.3 V) at 2.5 MHz

11 Power Supply Recommendations

The SN74AVC1T45 device uses two separate configurable power-supply rails, V_{CCA} and V_{CCB}. V_{CCA} accepts any supply voltage from 1.2 V to 3.6 V and V_{CCB} accepts any supply voltage from 1.2 V to 3.6 V. The A port and B port are designed to track V_{CCA} and V_{CCB} respectively allowing for low-voltage, bidirectional translation between any of the 1.2-V, 1.5 -V, 1.8-V, and 3.3-V voltage nodes.

11.1 Power-Up Considerations

A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies. To guard against such power-up problems, take the following precautions:

1. Connect ground before any supply voltage is applied.
2. Power up V_{CCA}.
3. V_{CCB} can be ramped up along with or after V_{CCA}.

Table 4. Typical Total Static Power Consumption (I_{CCA} + I_{CCB})

V_{CCB}	V_{CCA}						UNIT
	0 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
0 V	0	<0.5	<0.5	<0.5	<0.5	<0.5	μA
1.2 V	<0.5	<1	<1	<1	<1	1	
1.5 V	<0.5	<1	<1	<1	<1	1	
1.8 V	<0.5	<1	<1	<1	<1	<1	
2.5 V	<0.5	1	<1	<1	<1	<1	
3.3 V	<0.5	1	<1	<1	<1	<1	

12 Layout

12.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines are recommended:

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.
- Placing pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depending on the system requirements.

12.2 Layout Example

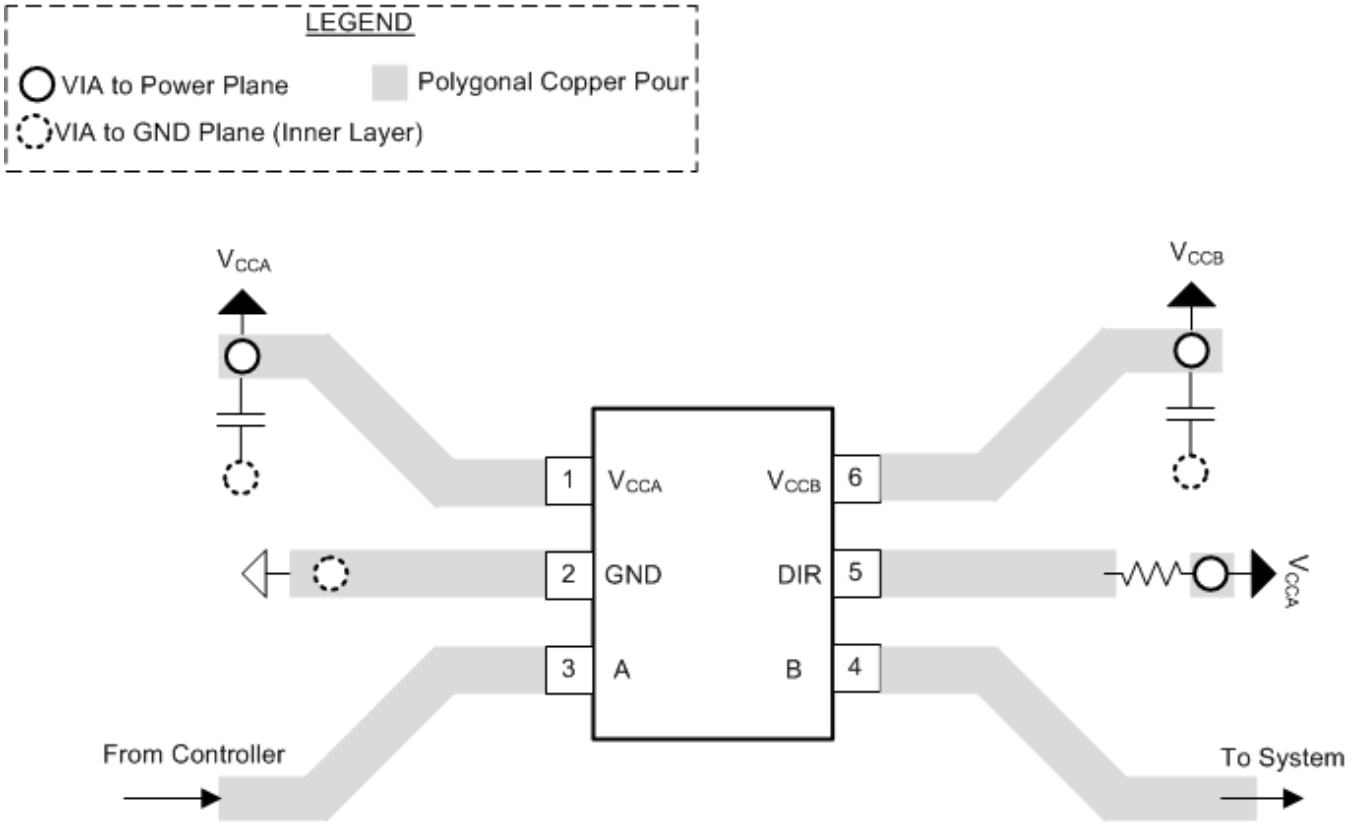


Figure 16. PCB Layout Example

13 Device and Documentation Support

13.1 Trademarks

NanoFree is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AVC1T45DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(DT1F, DT1R) (DT1H, DT1P)	Samples
SN74AVC1T45DBVRE4	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(DT1F, DT1R) (DT1H, DT1P)	Samples
SN74AVC1T45DBVRG4	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(DT1F, DT1R) (DT1H, DT1P)	Samples
SN74AVC1T45DBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	Call TI | NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT1R DT1H	Samples
SN74AVC1T45DBVTE4	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT1R DT1H	Samples
SN74AVC1T45DCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TCF, TCR) (TCH, TCP)	Samples
SN74AVC1T45DCKRE4	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TCF, TCR) (TCH, TCP)	Samples
SN74AVC1T45DCKRG4	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TCF, TCR) (TCH, TCP)	Samples
SN74AVC1T45DCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TCF, TCR) (TCH, TCP)	Samples
SN74AVC1T45DCKTG4	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TCF, TCR) (TCH, TCP)	Samples
SN74AVC1T45DRLR	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(1JW, TCR) TCH	Samples
SN74AVC1T45DRLRG4	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(1JW, TCR) TCH	Samples
SN74AVC1T45YZPR	ACTIVE	DSBGA	YZP	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(TC2, TCN)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

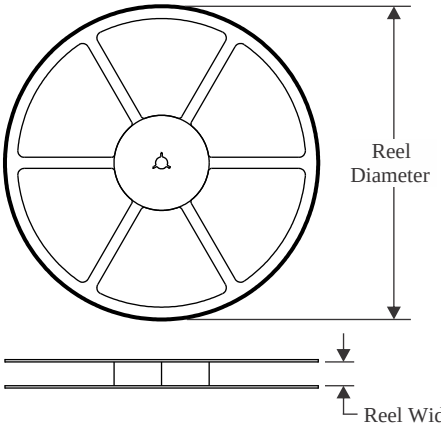
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

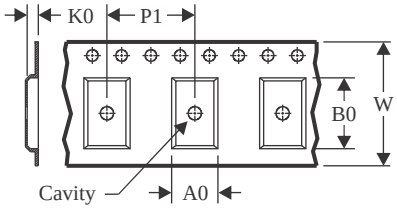
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

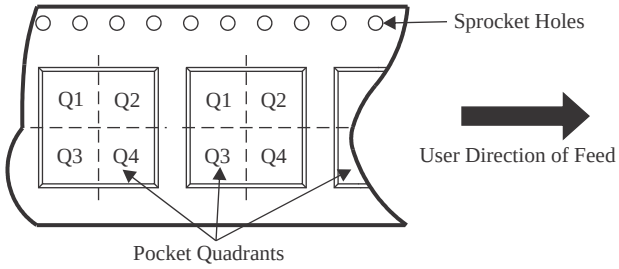


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

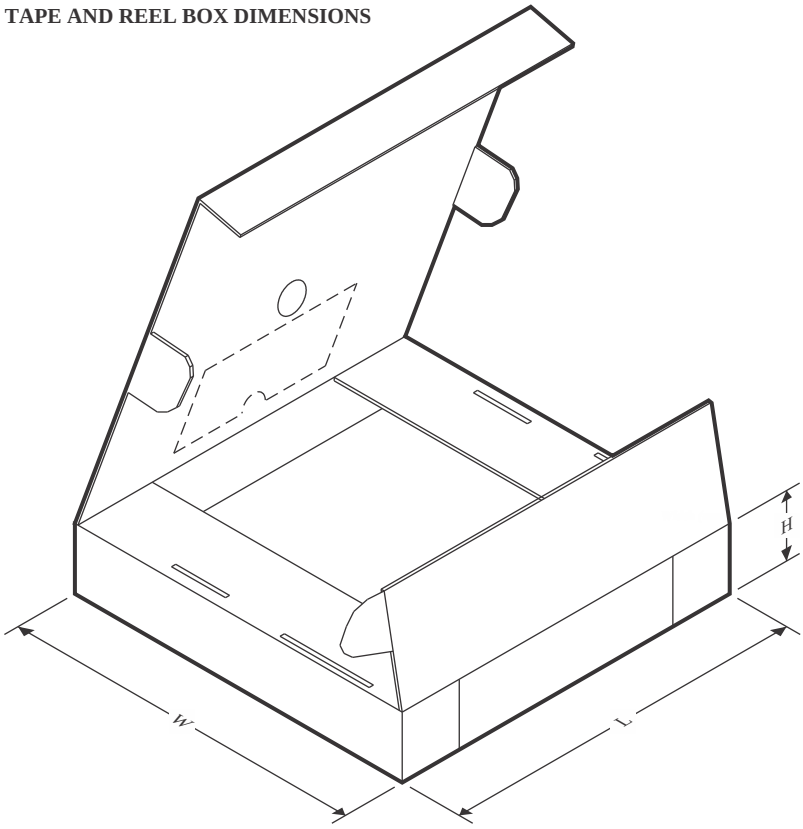
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVC1T45DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AVC1T45DBVT	SOT-23	DBV	6	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AVC1T45DCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74AVC1T45DCKT	SC70	DCK	6	250	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74AVC1T45DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74AVC1T45DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
SN74AVC1T45YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

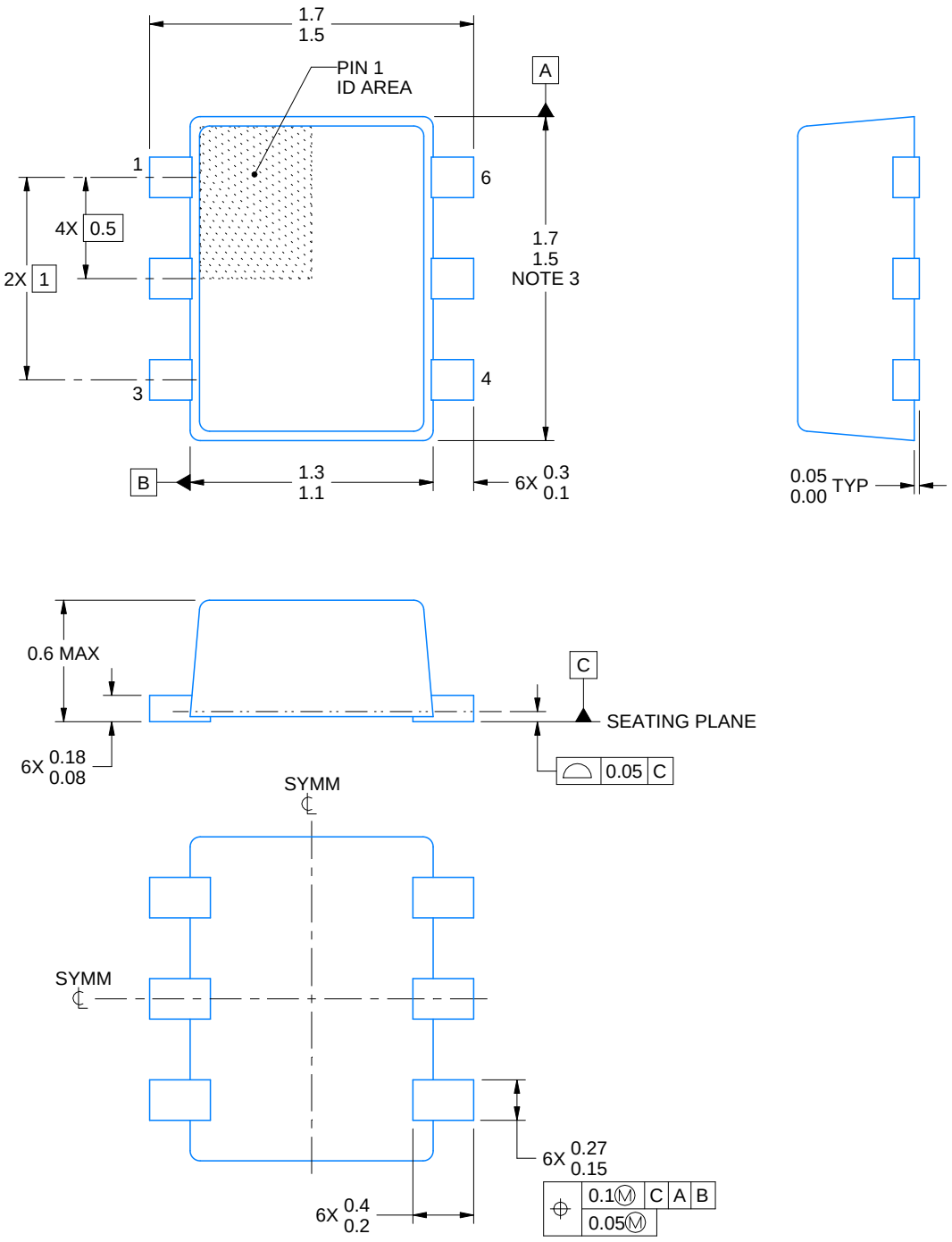
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVC1T45DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74AVC1T45DBVT	SOT-23	DBV	6	250	202.0	201.0	28.0
SN74AVC1T45DCKR	SC70	DCK	6	3000	202.0	201.0	28.0
SN74AVC1T45DCKT	SC70	DCK	6	250	202.0	201.0	28.0
SN74AVC1T45DRLR	SOT-5X3	DRL	6	4000	202.0	201.0	28.0
SN74AVC1T45DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
SN74AVC1T45YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

PACKAGE OUTLINE

DRL0006A

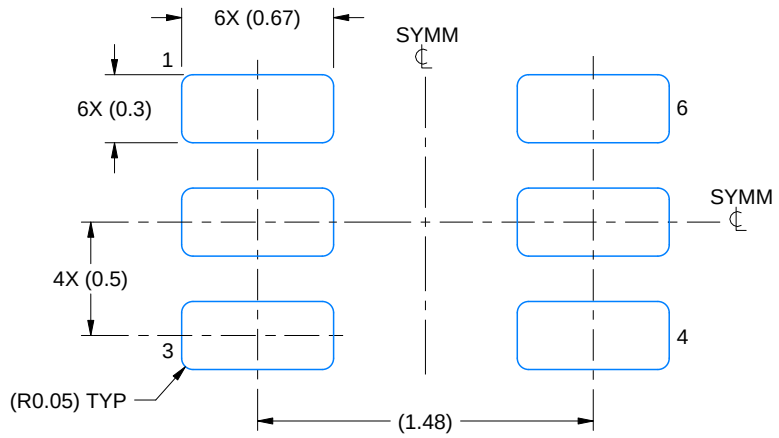
SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE

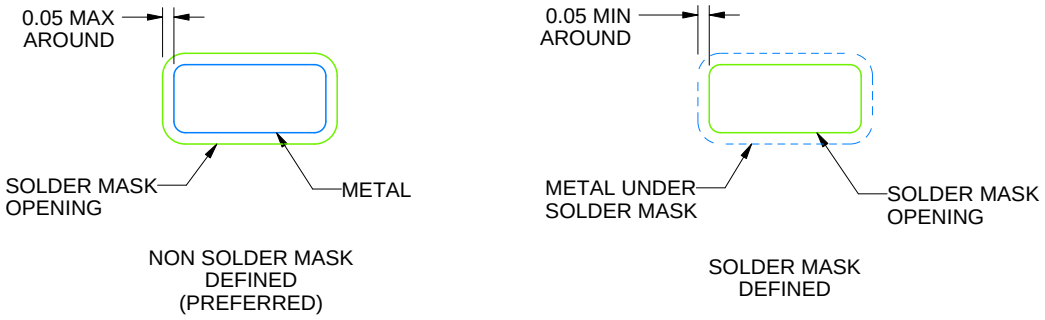


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4223266/C 12/2021

NOTES: (continued)

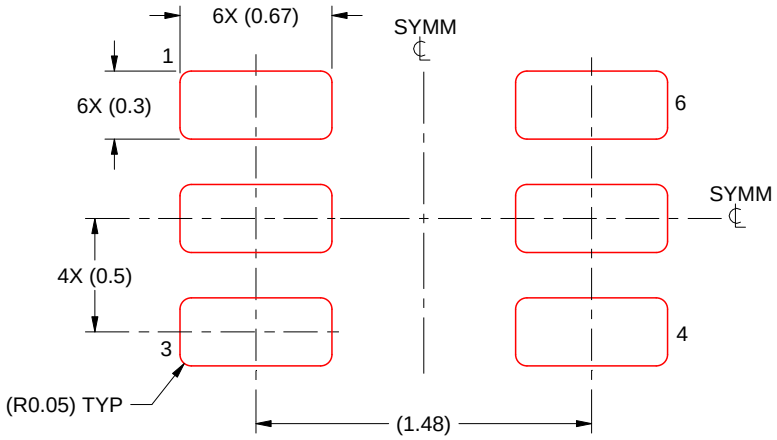
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/C 12/2021

NOTES: (continued)

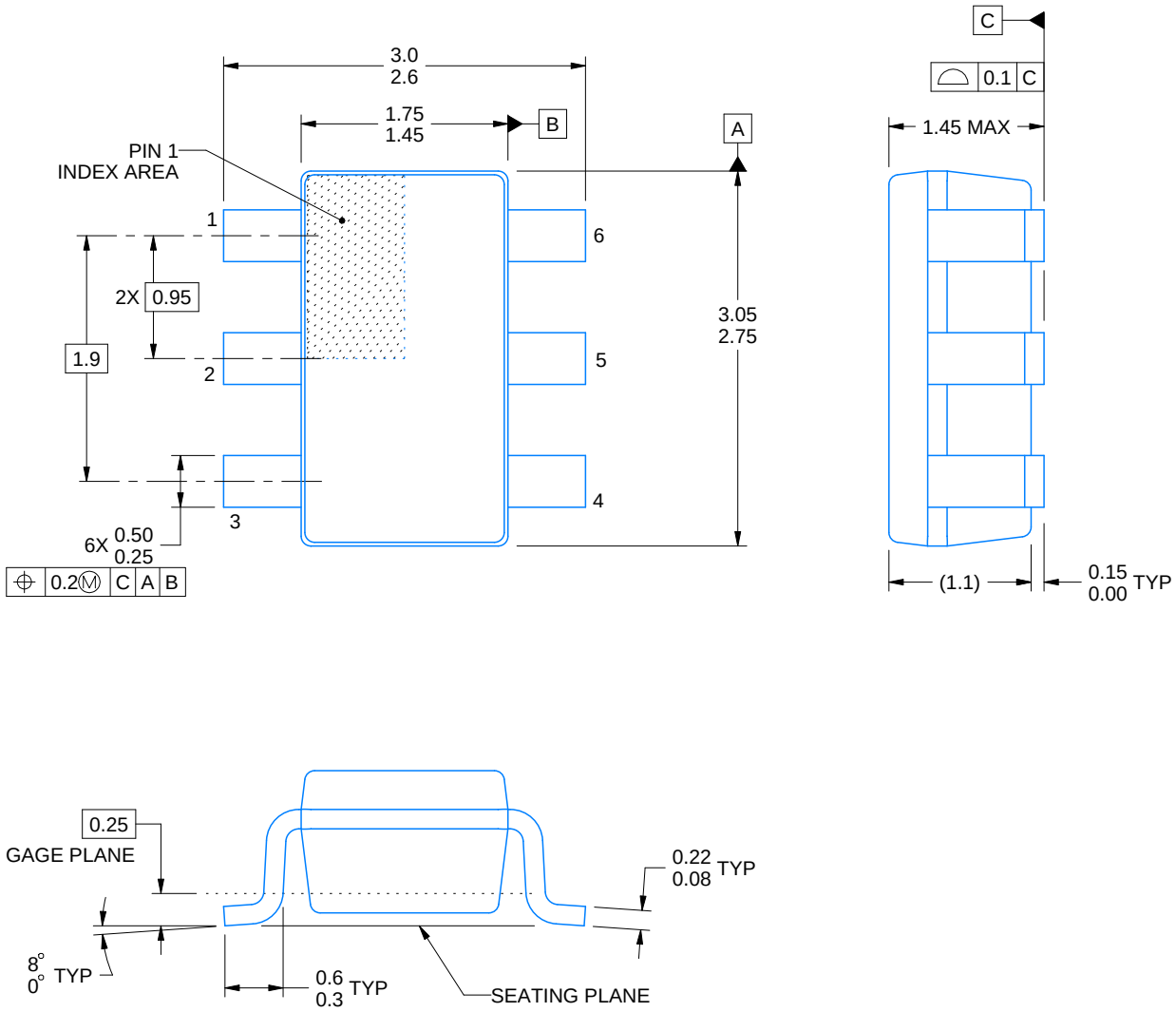
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

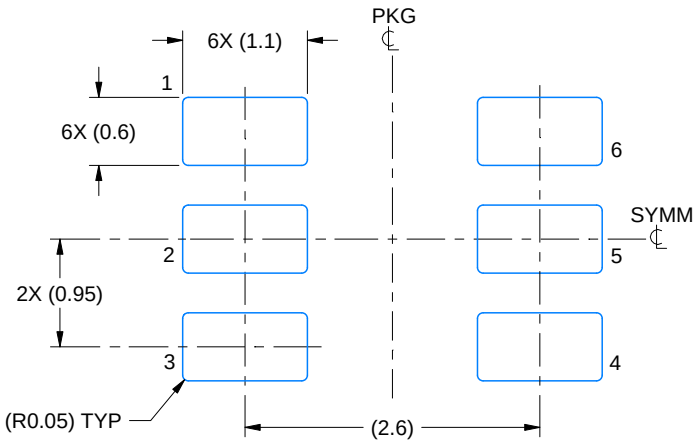
SMALL OUTLINE TRANSISTOR



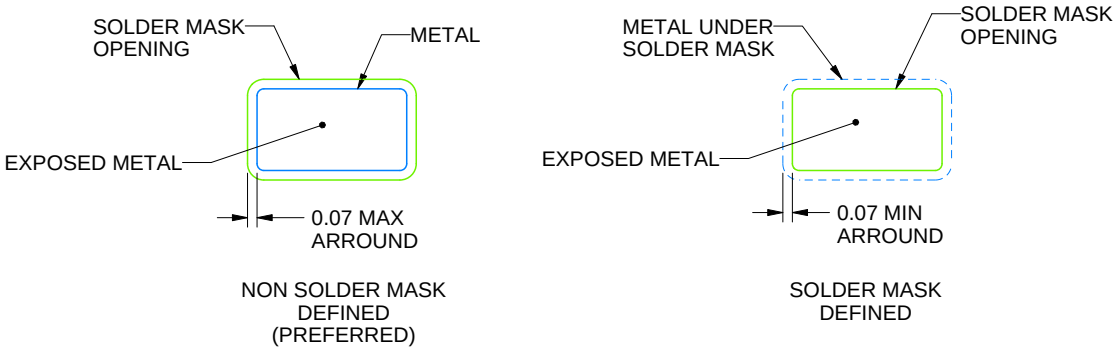
4214840/C 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

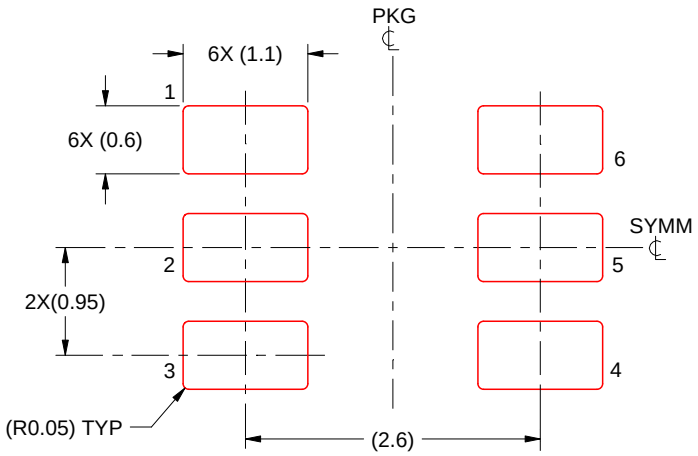


SOLDER MASK DETAILS

4214840/C 06/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/C 06/2021

NOTES: (continued)

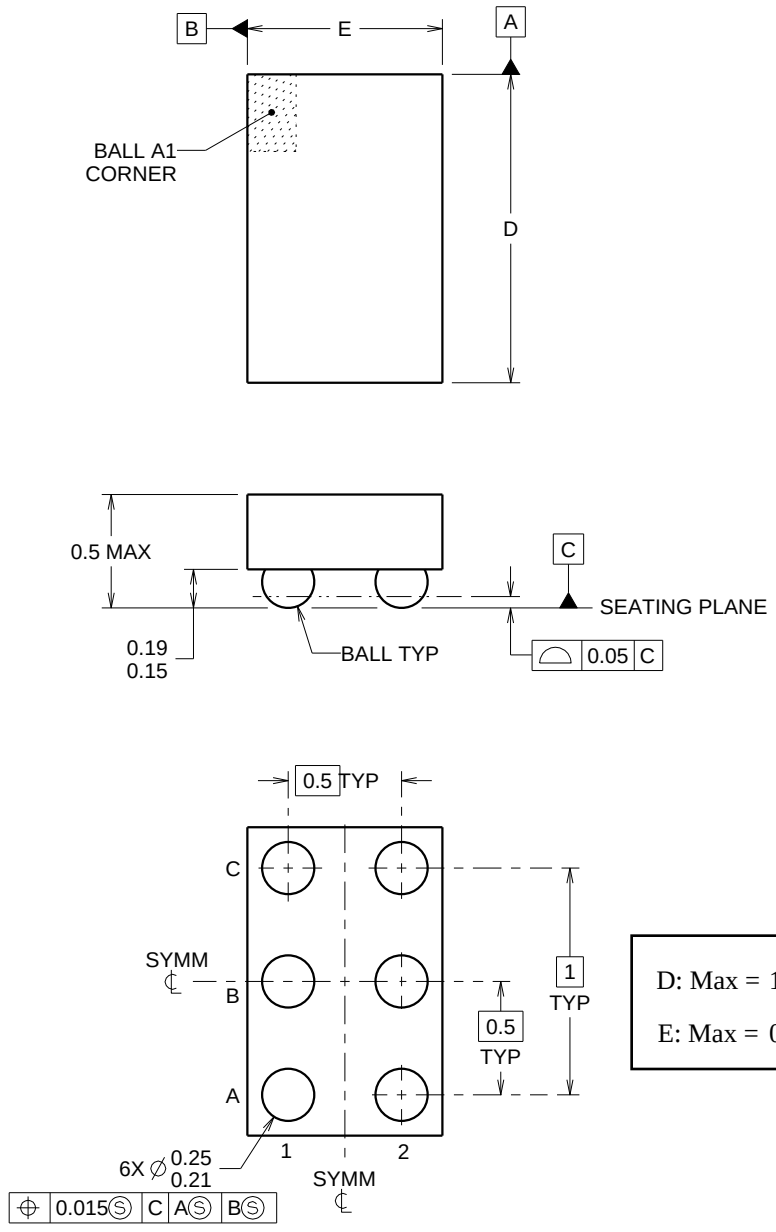
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.418 mm, Min =1.358 mm

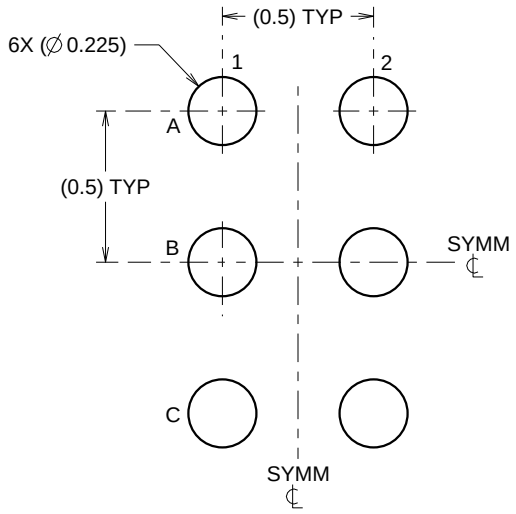
E: Max = 0.918 mm, Min =0.858 mm

4219524/A 06/2014

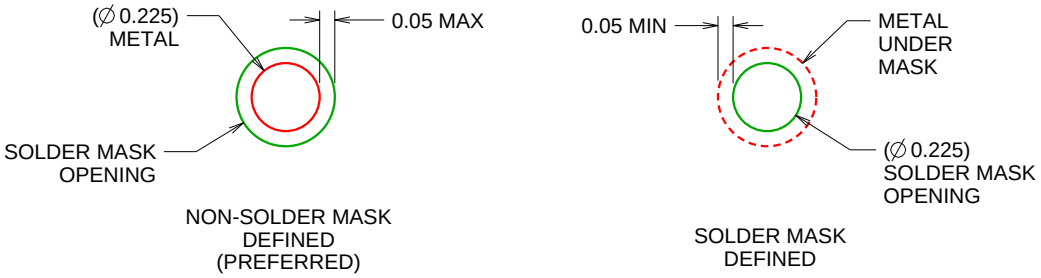
NOTES:

NanoFree Is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.



LAND PATTERN EXAMPLE
SCALE:40X

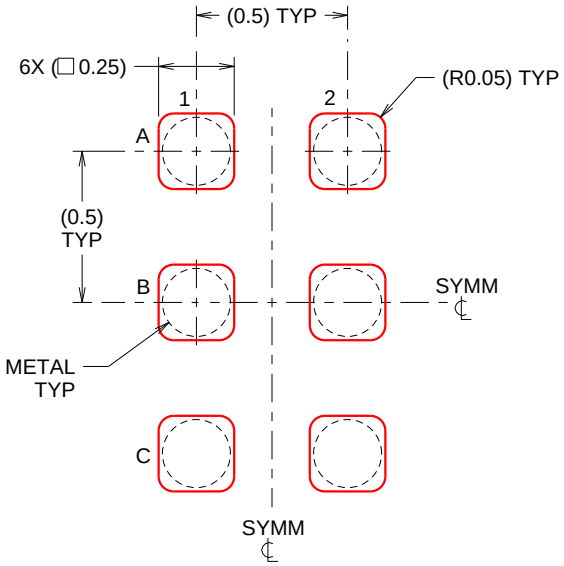


SOLDER MASK DETAILS
NOT TO SCALE

4219524/A 06/2014

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).



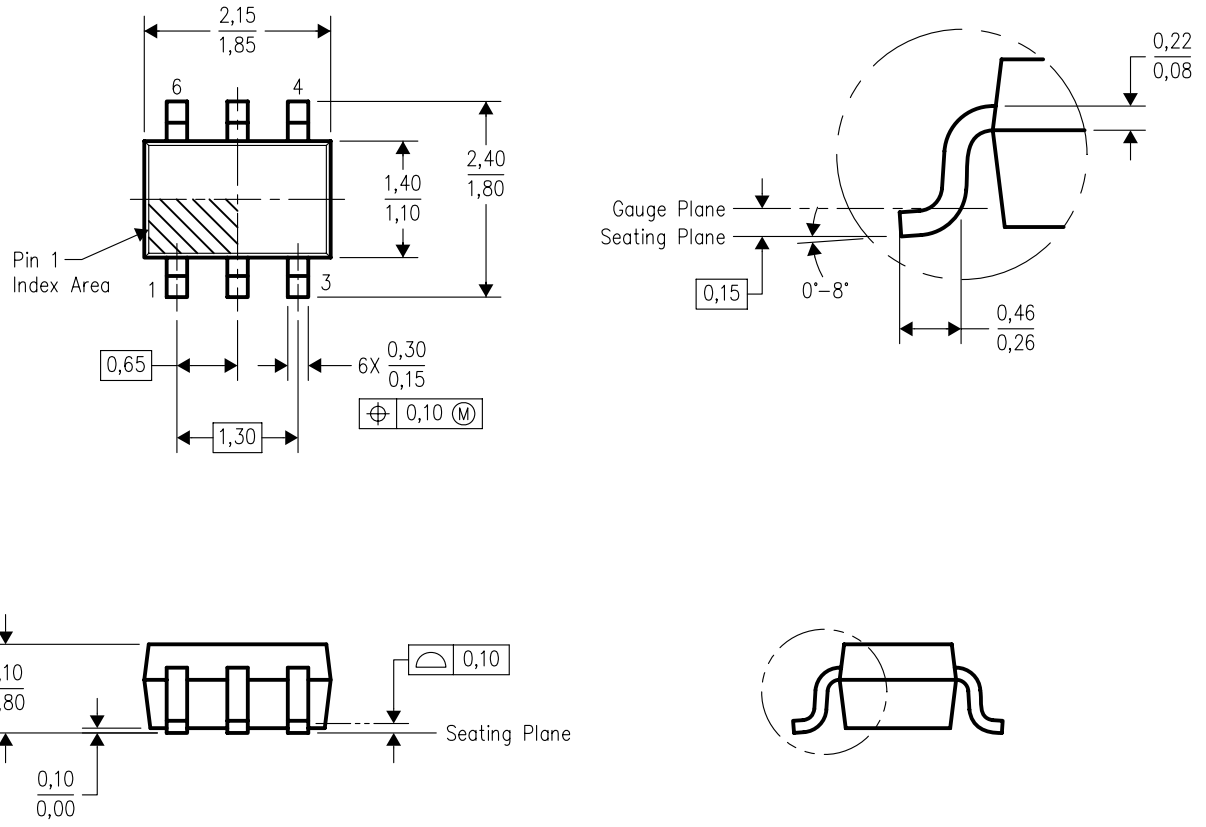
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

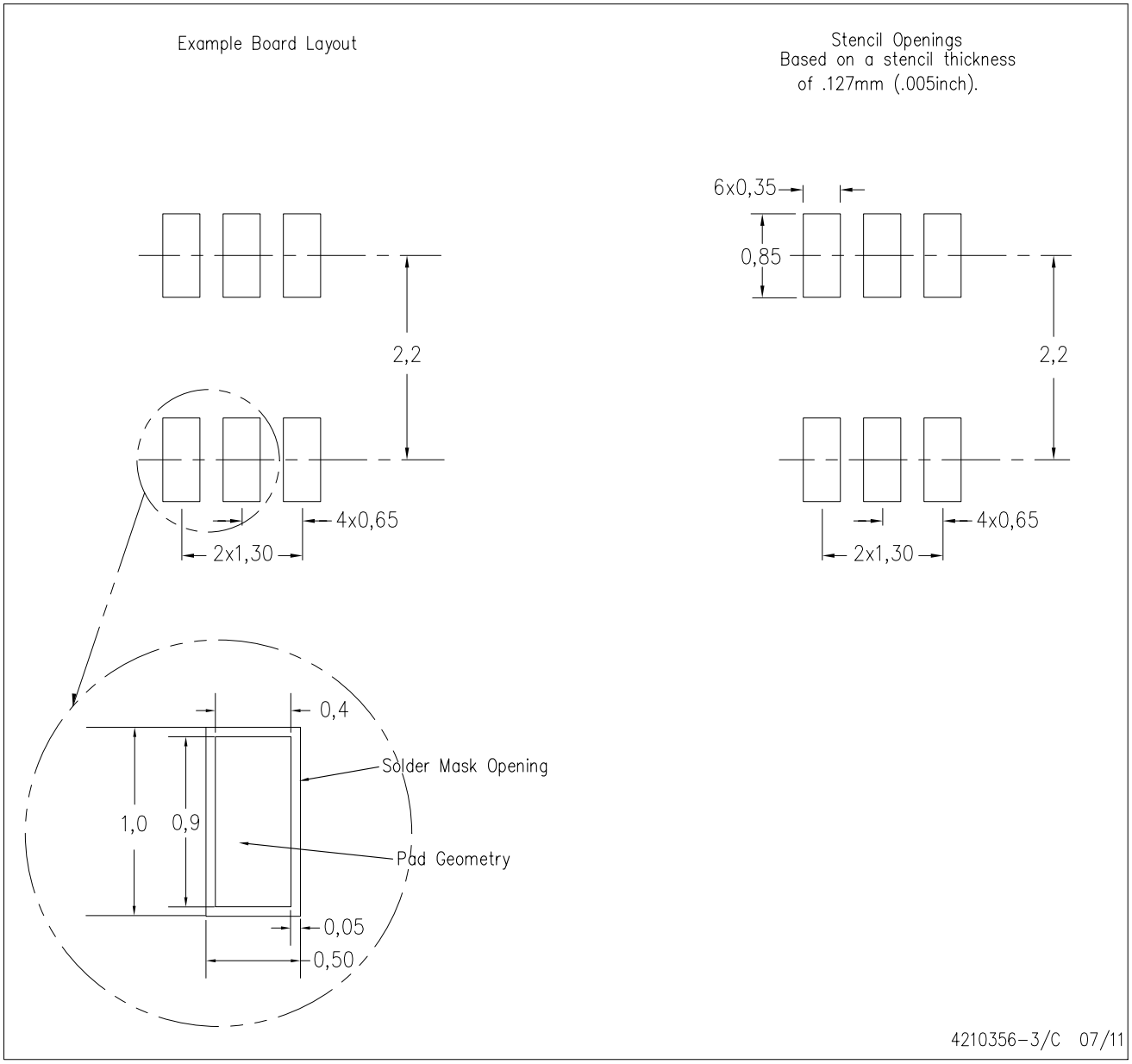
DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4093553–4/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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