Product Change Notification / SYST-20QISK339

Date:

24-Aug-2021

Product Category:

Interface- LIN Transceiver

PCN Type:

Document Change

Notification Subject:

Data Sheet - ATSAMHAXGXXA Data Sheet Document Revision

Affected CPNs:

SYST-20QISK339_Affected_CPN_08242021.pdf
SYST-20QISK339_Affected_CPN_08242021.csv

Notification Text:

SYST-20QISK339

Microchip has released a new Product Documents for the ATSAMHAXGXXA Data Sheet of devices. If you are using one of these devices please read the document located at ATSAMHAXGXXA Data Sheet.

Notification Status: Final

Description of Change:

1) Updated chapter DMA in DMAC Functional description. Removed reference to non-existent bit CHCTRLA.BURSTLEN.

2) Updated GPIO Clusters, removing duplicate entry. Fixed the link in the revision history for rev. B.

3) Fixed Reset Value of Register QOSCTRL in chapter DMAC

4) Fixed description of DRDY bit in register INTFLAG in I2C Client-mode to include data reception.

5) Clarified description of Standby mode with regards to RAM retention.

6) Fixed maximum clock frequency for DAC in Table Maximum Peripheral Clock Frequencies.

7) Fixed typo in the description of the bitfield EN32K in register OSC32K.

8) Removed reference to non-existent bit RUNSTDBY in the bit description of bit ONDEMAND in register DFLLCTRL.

9) Updated reset value in register LOCK in chapter NVMCTRL.

10) Corrected address and default value for the CPU QOS level.

11) Clarified behavior of Continuous read requests in chapter Read Request.

12) Corrected Properties of register DATA in chapter SERCOM I2C.

13) Updated bit description for RCONT in register READREQ in chapter TC.

14) Updated ADC block diagram to clarify in chapter ADC.

15) Added clarifying note in bitfield REFSEL in register REFCTRL in chapter ADC.

16) Clarified usage of register ADDR in chapter NVMCTRL.

17) Clarified clocking of RTC.

18) Clarified behavior of Pull-resistors when using pins in SERCOM - USART and SERCOM - SPI mode.

19) Updated BOD Reset diagram in chapter Elchar to clarify Reset behavior.

20) Updated Events and EVCTRL in chapter DAC to clarify DATA/DATABUF access.

21) Clarified SS pin depending on MSSEN state in bitfield DOPO in register CTRLA in chapter SERCOM - SPI.

22) Clarifications in Register CLKCTRL in GCLK

23) Clarifications in Register PCLKSR and PCLKSR in SYSCTRL. Fixed reset values for B33SRDY, BOD33RDY, DFLLRDY, OSC8MRDY.

24) Fixing properties in Registers DATA and DATABUF in DAC.

25) The SPI and I2C standards use the terminology "Master" and "Slave". The equivalent Microchip terminology used in this document is "Host" and "Client" respectively. These terms have been updated throughout this document for this revision.

26) The LIN standards use the terminology "Master" and "Slave". The equivalent Microchip terminology used in this document is "Commander" and "Responder" respectively. These terms have been updated throughout this document for this revision.

27) Fixed and added Links in rev. history B

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 24 Aug 2021

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

ATSAMHAXGXXA Data Sheet

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Affected Catalog Part Numbers (CPN)

ATSAMHA0G14A-MZT-BVAO
ATSAMHA0G15A-MZT-BVAO
ATSAMHA0G16A-MZT-BVAO
ATSAMHA1G14A-MBT
ATSAMHA1G14A-MBT-BVAO
ATSAMHA1G15A-MBT
ATSAMHA1G15A-MBT-BV02
ATSAMHA1G15A-MBT-BV07
ATSAMHA1G15A-MBT-BVAO
ATSAMHA1G16A-MBT
ATSAMHA1G16A-MBT-BV01
ATSAMHA1G16A-MBT-BV03
ATSAMHA1G16A-MBT-BV04
ATSAMHA1G16A-MBT-BVAO